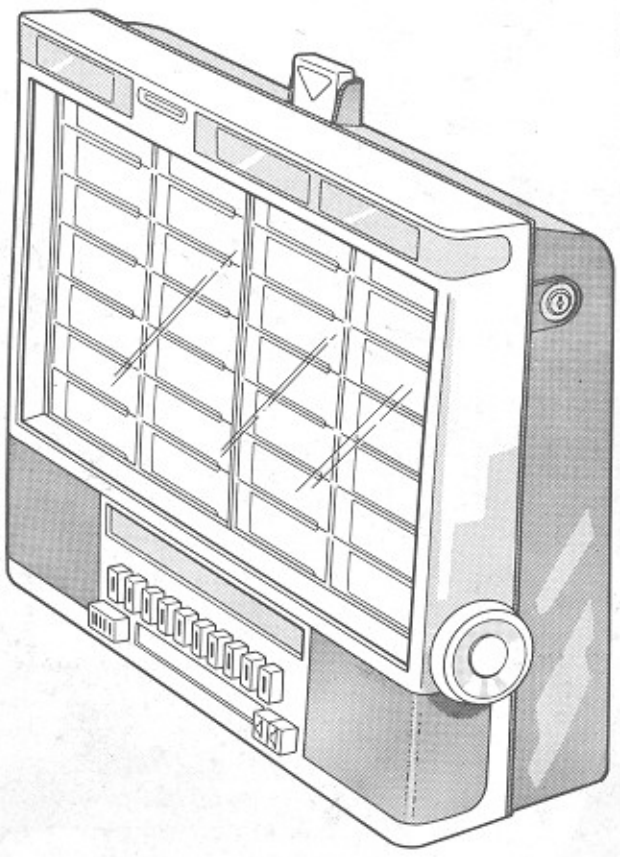
SERVICE MANUAL AND PARTS CATALOG

ROCK-OLA

TRI-VUE STEREO WALL BOX

MODEL 506



WALL BOX PULSE SEQUENCE

SELECTION NUMBER	1st Pulse Train	2nd Pulse Train
100	2	1
200	3	1
110	4	1
210	5	1
120	6	1
220	7	1
130	8	1
230	9	1
140	10	1
240	11	1
150	12	1
250	13	1
160	14	1
260	15	1
170	16	1
270	17	1
180	18	1
280	19	1
190	20	1
290	21	1

SELECTION NUMBER	1st Pulse Train	2nd Pulse Train
102	2	3
202	3	3
112	4	3
212	5	3
122	6	3
222	7	3
132	8	3
232	9	3
142	10	3
242	11	3
152	12	3
252	13	3
162	14	3
262	15	3
172	16	3
272	17	3
182	18	3
282	19	3
192	20	3
292	21	3

SELECTION NUMBER	1st Pulse Train	2nd Pulse Train
104	2	5
204	3	5
114	4	5
214	5	5
124	6	5
224	7	5
134	8	5
234	9	5
144	10	5
244	11	5
154	12	5
254	13	5
164	14	5
264	15	5
174	16	5
274	17	5
184	18	5
284	19	5
194	20	5
294	21	5

SELECTION NUMBER	1st Pulse Train	2nd Pulse Train
106	2	7
206	3	7
116	4	7
216	5	7
126	6	7
226	7	7
136	8	7
236	9	7
146	10	7
246	11	7
156	12	7
256	13	7
166	14	7
266	15	7
176	16	7
276	17	7
186	18	7
286	19	7
196	20	7
296	21	7

101	2	2
201	3	2
111	4	2
211	5	2
121	6	2
221	7	2
131	8	2
231	9	2
141	10	2
241	11	2
151	12	2
251	13	2
161	14	2
261	15	2
171	16	2
271	17	2
181	18	2
281	19	2
191	20	2
291	21	2

103	2	4
203	3	4
113	4	4
213	5	4
123	6	4
223	7	4
133	8	4
233	9	4
143	10	4
243	11	4
153	12	4
253	13	4
163	14	4
263	15	4
173	16	4
273	17	4
183	18	4
283	19	4
193	20	4
293	21	4

105	2	6
205	3	6
115	4	6
215	5	6
125	6	6
225	7	6
135	8	6
235	9	6
145	10	6
245	11	6
155	12	6
255	13	6
165	14	6
265	15	6
175	16	6
275	17	6
185	18	6
285	19	6
195	20	6
295	21	6

107	2	8
207	3	8
117	4	8
217	5	8
127	6	8
227	7	8
137	8	8
237	9	8
147	10	8
247	11	8
157	12	8
257	13	8
167	14	8
267	15	8
177	16	8
277	17	8
187	18	8
287	19	8
197	20	8
297	21	8

WALL BOX MODEL 506

GENERAL INFORMATION

The audio type Model 506 Wall Box is a digital electronic version of its electro-mechanical predecessors and operates with either a 160 selection or 100 selection phonograph. Although the Model 506 Wall Box selection system operates on a 3 digit numerical code, the principle of transmitting electrical information to the receiver remains the same and can be intermixed with previous model wall boxes, receivers and phonographs.

As you read this Service and Operating Instruction Manual, you will notice steps which have been incorporated in its layout to present the operation of the Model 506 to you in the simplest manner possible.

Through graphics consisting of line drawings and schematics, this manual will visually and verbally take you step by step through all the electrical and mechanical actions involved in the operation of the Model 506.

All operations are in their actual sequences and all parts and electrical circuits involved in these sequences are clearly demonstrated. A few hours spent with this manual studying the operation will thoroughly acquaint you with its operation. Should there be a need for more information, your Rock-Ola distributor or the Rock-Ola factory service organization is always available to assist.

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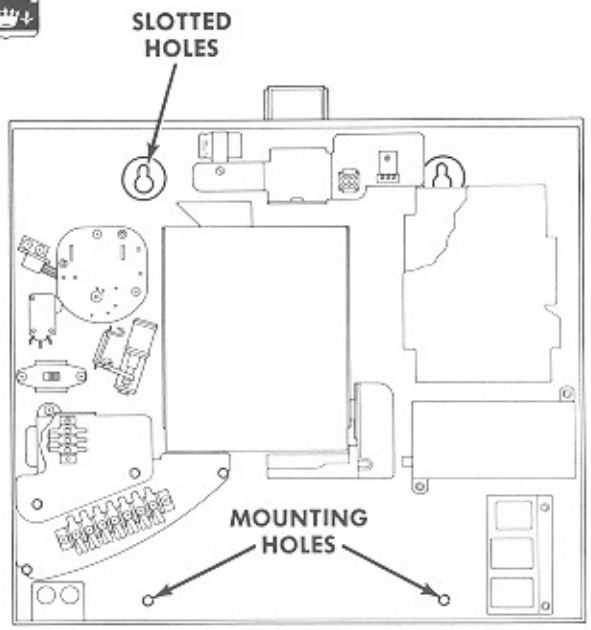
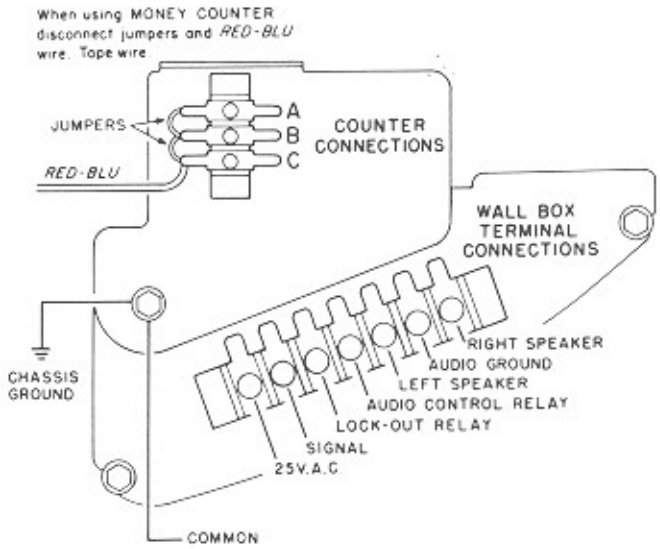




MOUNTING THE WALL BOX

A Wall Box Mounting Plate is provided for rigidly mounting the Wall Box on the wall or Bar Brackets, Kit. No. 2149.

For wall installations hang the mounting plate over a nail already set at the proper height.

Level and mark the two top and two bottom corner holes. Use the four mounting points for anchoring, it may be necessary to shim the plate if the wall is uneven. Place two nuts on the upper two mounting studs.

On the Wall Box back plate there are four holes for mounting over the four mounting studs. The upper two are slotted for placing over the top studs with the nuts. The two lower holes is for rigid mounting after the wall box has been hung in place.

Unlock the Wall Box and remove the cash box. Place nuts over the two bottom mounting studs and tighten the four nuts.

WIRING THE WALL BOX

A ll wire interconnecting cable is required which should not be smaller than #18 gauge (for each wire) in order that the voltage drop from the phonograph to the wall box be kept to a minimum.

Note: Color code matching must be strictly observed between wall box and phonograph terminal connections.

Four wires are required to supply power to the wall box. Solder each lead. Two of the four wires supply 25 V.A.C. The third wire is an overlapping lock-out circuit from the receiver to the lockout relay. The fourth wire constitutes the signal circuit that keys the receiver unit.

Four wires are required to operate the wall box audio system. Three of the wires operate the left and right channel speakers. The fourth wire establishes a locking circuit from the phonograph to the audio control relay in the wall box. This allows speakers to be "on" in that particular wall box that is registering a selection. The wall box volume control is controlled by the customer thru the use of two external volume control pushbutton switches.

The last three wires are coin counting circuits from the wall box to the wall box Adapter Kit No. 1995-2 mounted on the Coin Counter Kit No. 1989-2. This equipment is optional.

The other end of the inter-connecting cable is connected to the phonograph terminal strip located below the rear door.

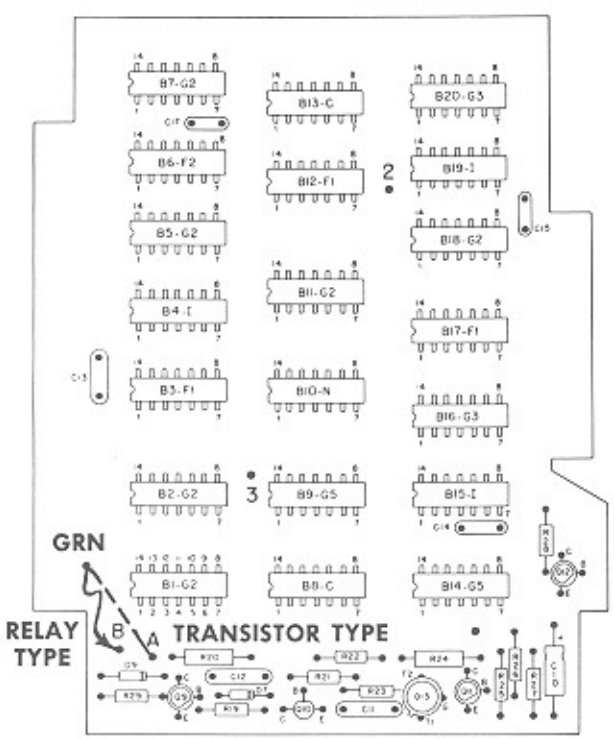
AUXILIARY POWER SUPPLY

The 25 volt signal transformer in the Receiver is capable of supplying power to ten (10) wall boxes. Using more than this number without an auxiliary power supply, Kit No. 2121, may result in burning out the 3 ampere fustat on the Receiver unit, or the prolong heating of the transformer may cause it to fail.

WALL BOX ADJUSTMENTS

Receiver Consideration

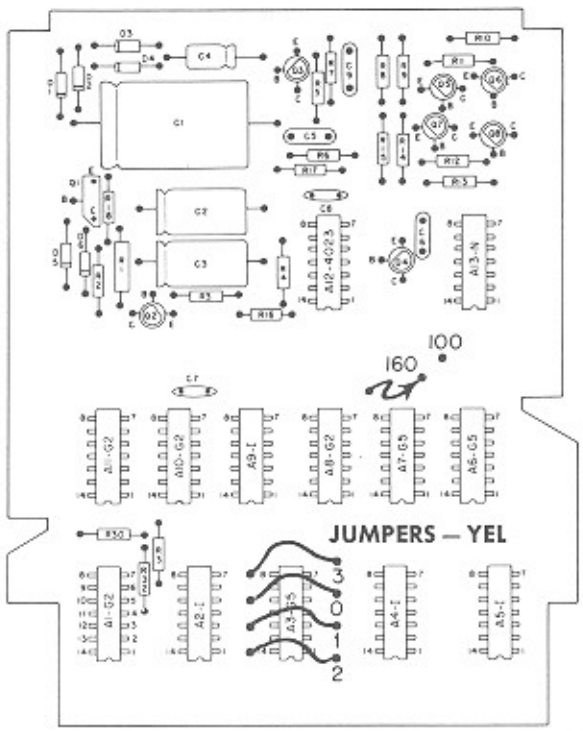
The Wall Box is initially set to operate in conjunction with a transistorized Receiver starting with Model 1765-2. To operate the Wall Box with a relay type Receiver (Model 1765 and prior), move the jumper on the top P.C. Board from position "A" to position "B". See figure below.



P.C. BOARD No.2 (TOP)

Album/Singles Programming

When the Wall Box is shipped, the four Album/Singles jumpers are connected setting up the system for "Singles" play only.



P.C. BOARD No.1 (BOTTOM)

Each jumper when removed represents a Album group of 20 selections ending with the 3rd Digit number 0–1–2 or 3. Album programming should be made in numerical order.

The pricing system is preset to accept Quarters and Half-Dollars only. Nickels and Dimes are returned to the customer.

The credit equipment includes a Quarter Credit Alternator which permits a 2–3–2–3 credit incentive arrangement.

Quarters and Half-Dollars are set to the following credit value.

PRICE	SINGLES	ALBUM
Quarter	2	1
2 Quarters or Half-Dollar	5	plus 1 single

Credit System Pricing Adjustment

To accommodate requirements for Standard Play of 10¢–25¢–50¢ pricing, do the following:

1. Remove 50¢ Rejector. Reset nickel and dime adjustments to accept these coins.

2. Adjust center accumulator ratchet (50¢) to a 7 credit position.

3. Adjust outer ratchet (25¢) to a 3 credit position.

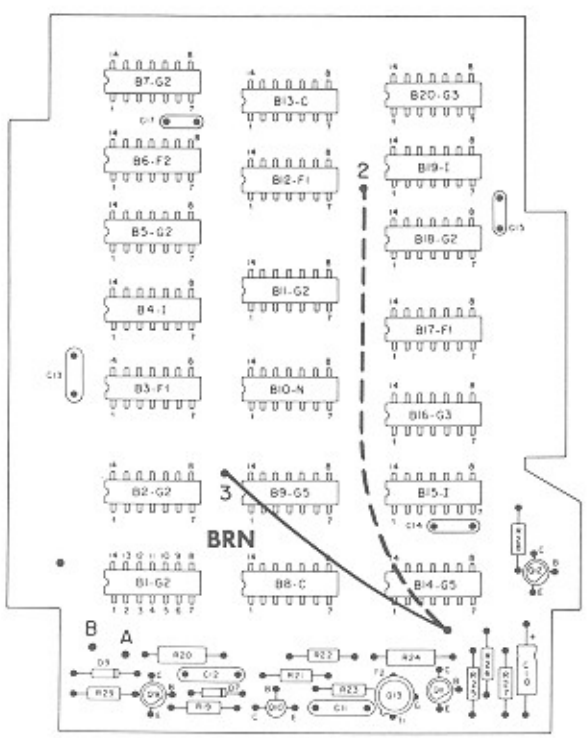
4. Adjust Album Credit Switch to "click" between the 2nd and 3rd tooth when 3 or more credits register.

5. Move 2/3 Quarter Adapter switch to "STD" position.

   Note: Pricing adjustments Step 1 thru Step 5 are alike for Wall Box and Phonograph. These adjustments are illustrated on the Credit System Pricing Adjustment sheet included with the Phonograph Service Material.

6. Move the jumper on the top P.C.Board from the 2 Credit Pin to the 3 Credit Pin.

   New Pricing Cards are included with the Wall Box.



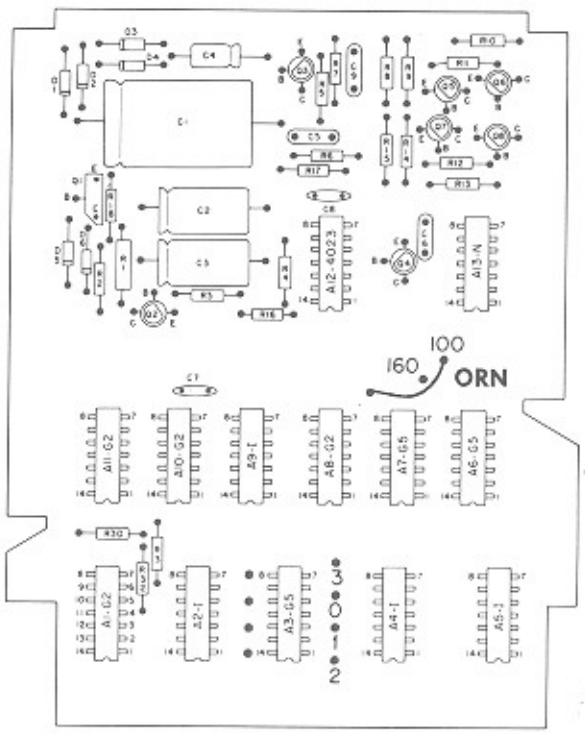
P.C. BOARD No.2 (TOP)

Audio Power Consideration

Refer to the Speaker Installation Guide label located on the back door of the phonograph.

Wall Box Adjustment for 100 Selection Operation

The Wall Box as shipped from the factory is preset for 160 selection operation. To convert the Wall Box for 100 selection operation, two adjustments are necessary.



P.C. BOARD No.1 (BOTTOM)

The 1st adjustment is made on the bottom P.C. Board. Move jumper from "160" position to "100". The new position of the jumper disables circuits to the last 60 selections and if selected will cause the Reset & Reselect lamp to turn on.

The 2nd adjustment is made on the Program Holder Assembly. Remove Program Holder from Wall Box. See Fig. A.

Turn program knob until the key-way on the program holders faces the front. Transpose the position of the Program Lock-out Plate. This adjustment will allow only two sides of the program holders to be turned into viewing position. See Fig. B.

Insert Filler Strips (included with the Wall Box) on the 2nd viewing side for selections (105-205), (115-215), (125-225) and (135-235). See Fig. C.

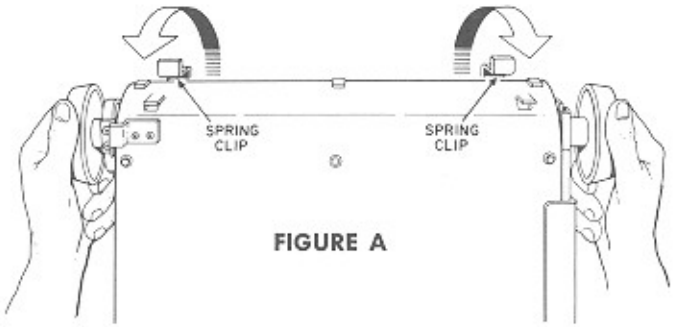


FIGURE A

PROGRAM HOLDER REMOVAL

The Program Holder is secured inside the front housing by two spring clips. Lift the program holder upward to remove. Hold spring clips open if necessary.

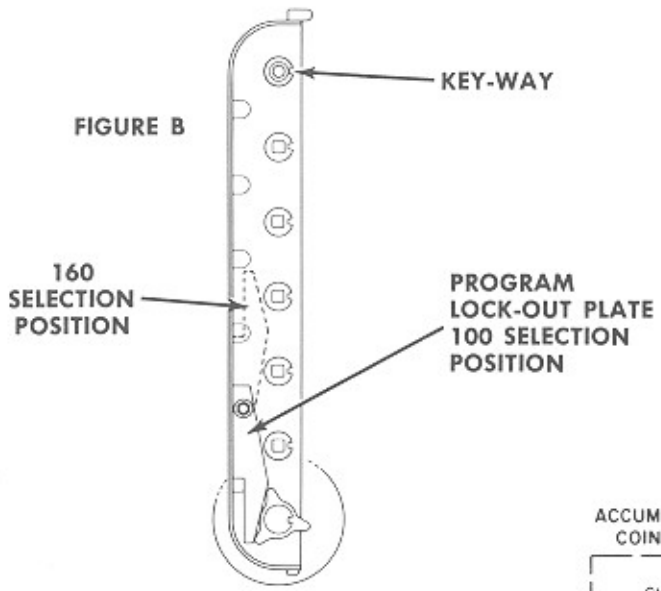


FIGURE B

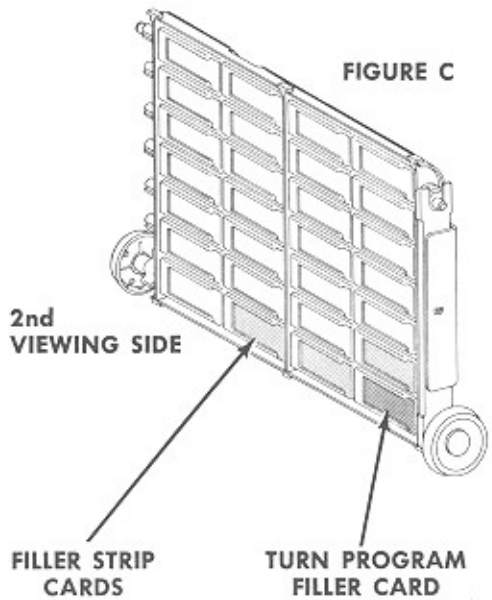


FIGURE C

WALL BOX 2/3 QUARTER ADAPTER

General Information

The adapter is activated upon insertion of Quarters only.

Cycle Of Operation

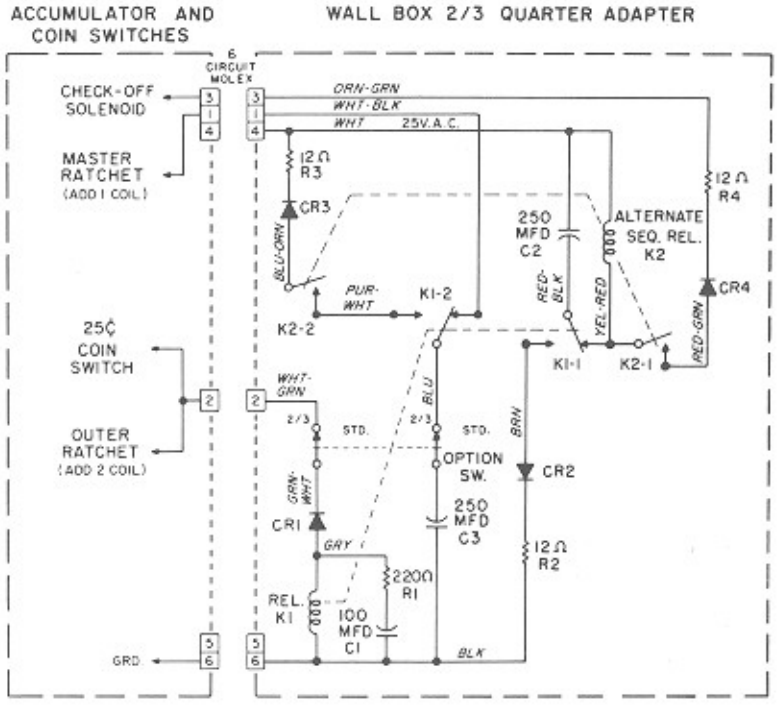
1. Down stroke of the quarter coin switch allows accumulator quarter ratchet to register 2 credits; relay K1 energizes and C1 charges thru CR1 and R1.

2. Relay contacts K1-1 and K1-2 transfer, C2 charges thru CR2 and R2.

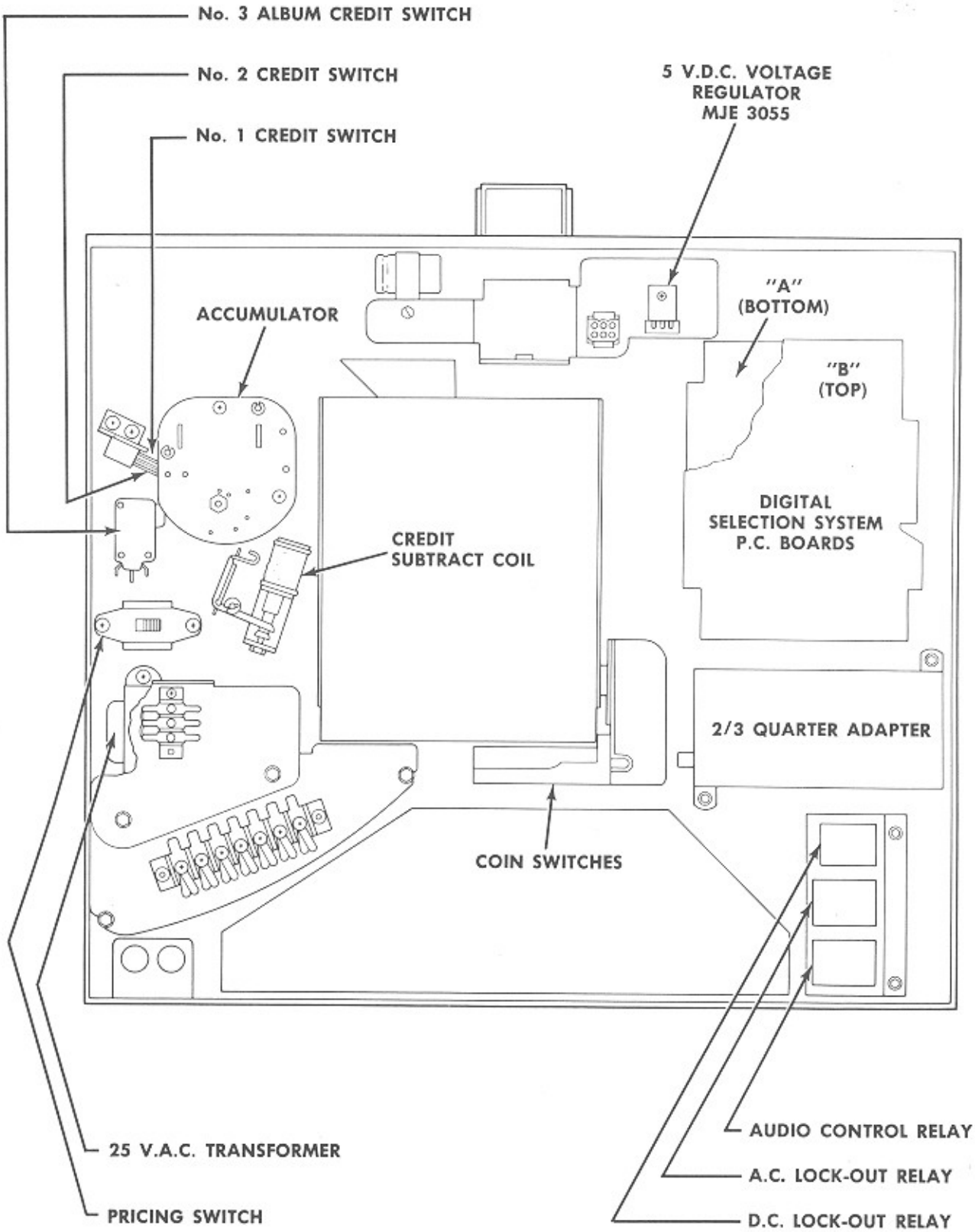
3. Coin switch opens. After a short delay due to C1 discharging thru R1 and K1 coil, K1 relaxes. C2 discharges thru relaxed K1-1 and operates the sequence relay K2. Relay K2 relaxes and relay contacts K2-1 and K2-2 close.

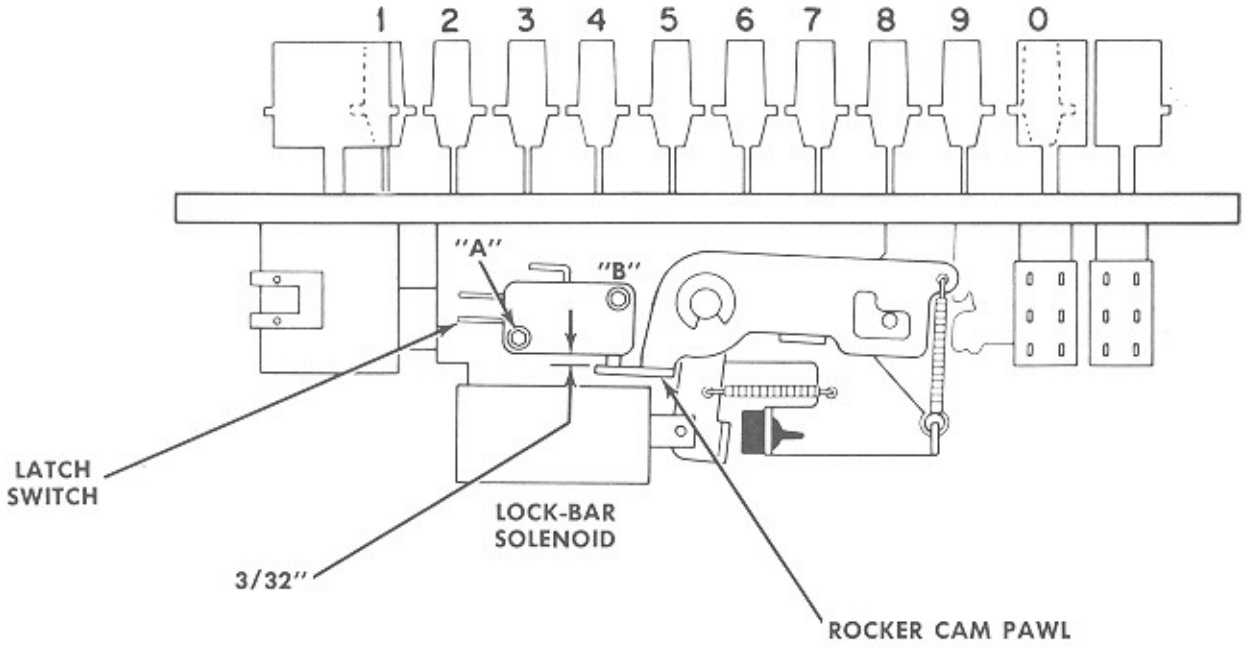
4. Steps #1 thru #3 are repeated as quarter coin switch closes a second time except that C3 charges thru closed K2-2. When K1 relay relaxes, C3 discharges thru K1-2, momentarily operating the master ratchet "Add 1" coil in addition to the sequence relay K2. When K2 relaxes, contacts K2-1 and K2-2 open.

5. RESET–If at any time, a selection is made and the sequence relay contacts K2-1 and K2-2 are closed, the sequence relay operates thru R4 and CR4 from the next subtract solenoid pulse. This causes K2-1 and K2-2 contacts to open and result in an "Add 2" only condition upon the next operation of the quarter coin switch.



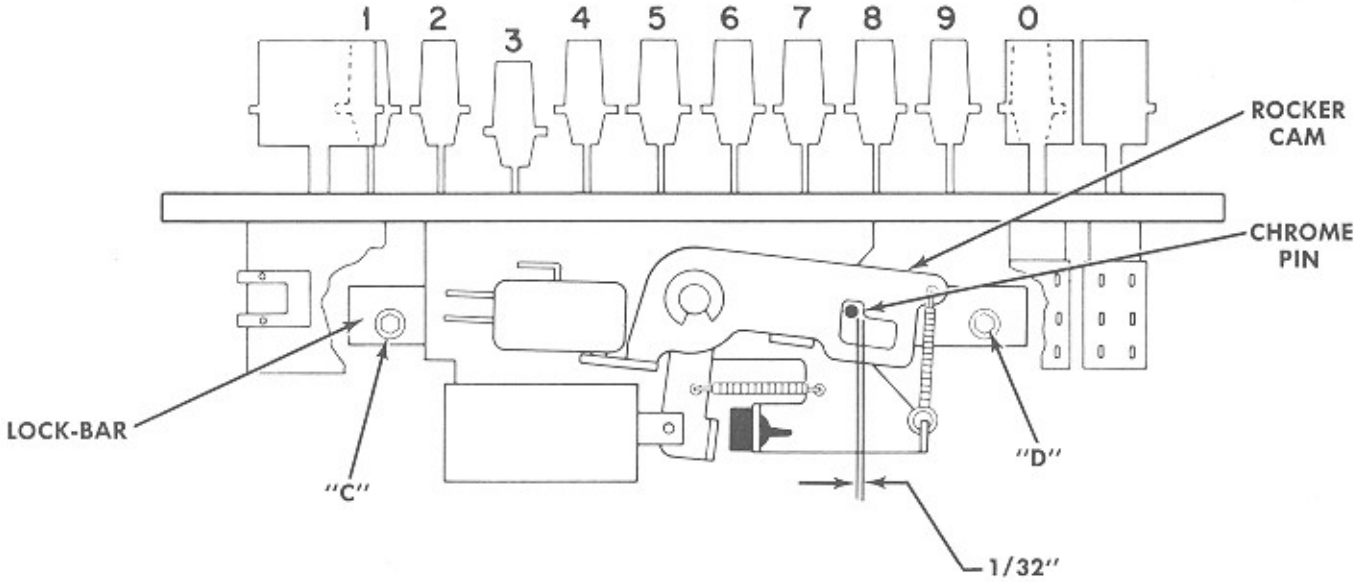
OPERATING ELEMENTS OF THE WALL BOX





LATCH SWITCH ADJUSTMENT

With a energized Lock-Bar Solenoid the air gap between the Rocker Cam Pawl and Latch Switch should be 3/32". Loosen screws "A" and "B" and adjust switch accordingly.



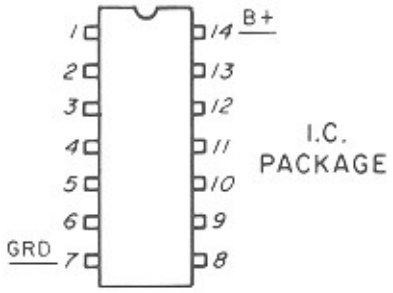
SELECTION BUTTON LOCKING ADJUSTMENT

With a energized Lock-Bar Solenoid and the 3rd Digit Selection Number pressed in fully, loosen screws "C" and "D". Adjust Lock-Bar for 1/32" overtravel between the Rocker Cam and Chrome Pin.

DIGITAL SELECTION SYSTEM

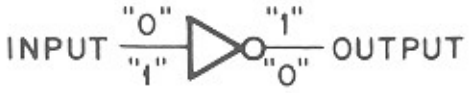
The selection system consists of logic elements that are contained in 33 intergrated circuits or packages. There are 9 types of which 7 are used in two or more places. The logic elements used are INVERTERS, ... NAND gates, ... NOR gates, ... FLIP-FLOPS and Counters.

I.C. Type	Number Used
INVERTER	7
2 input NAND gate	10
3 input NAND gate	2
5 input NAND gate	5
NOR gate	2
F1 FLIP-FLOP	3
F2 FLIP-FLOP	1
Counters	2
Divide Counters	1



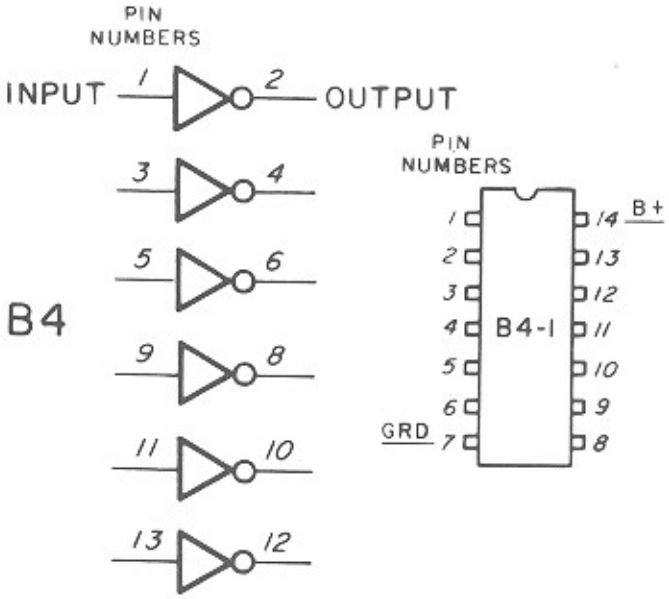
Each I.C. has 14 pin connections. Pin 7 is used for ground and Pin 14 for B+. The remaining 12 pins are used for input and output circuits.

INVERTER



Symbol

The INVERTER logic element has 1 input and 1 output. A "O" signal (less than .5 volt) when applied to the input causes the output to become "1" (3.6 to 5 volts) or, ... a "1" signal applied to the input, the output becomes "O".



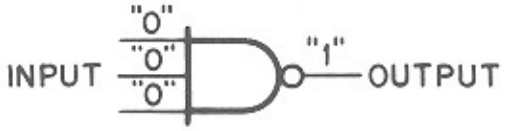
A INVERTER I.C. contains 6 INVERTER elements. Each I.C. is coded alpha-numerically, as B4-1, and each element input and output is designated by a pin number.

Letter "B" indicates that the I.C. is located on the Top P.C. Board, ... letter "A", on the Bottom P.C. Board. Numeral "4" pin points the I.C. location, ... the "I" for INVERTER. All I.C. packages on the P.C. Boards and Schematics are designated in this manner.

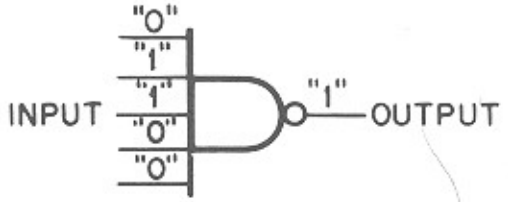
NAND gates

The NAND gate elements used in the system are either a 2 input, ... 3 input, ... or a 5 input type.

2 input NAND gate Symbol



3 input NAND gate Symbol

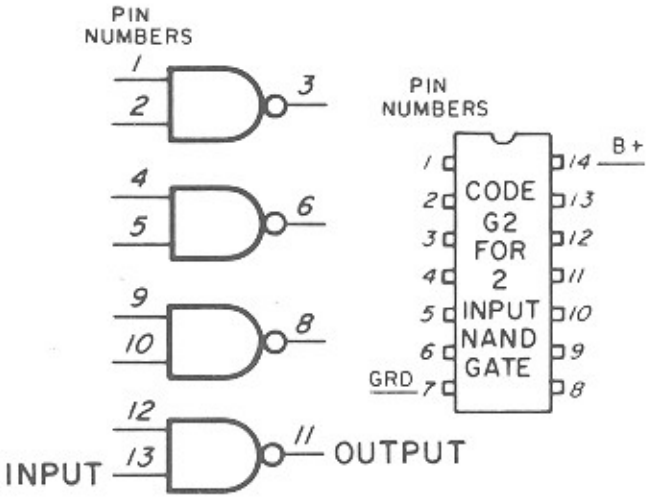


5 input NAND gate Symbol

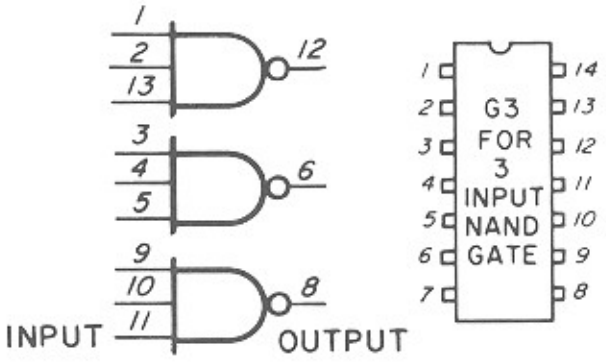
The NAND gate outputs will be "O" only if all inputs are "1" or, . . . if all inputs are "O", outputs will be "1".

Any combination of "O" and "1" on the inputs, the outputs will remain "1".

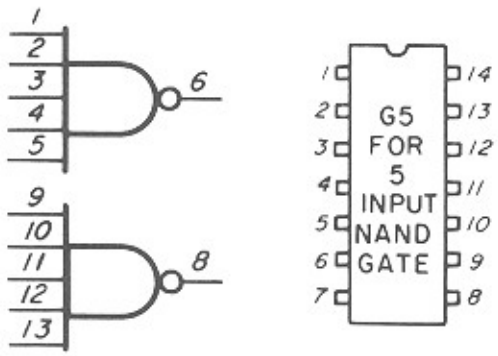
There are 4 NAND gate elements of the 2 input type that are packaged into one I.C.



The 3 input type NAND gate has 3 elements packaged into one I.C.



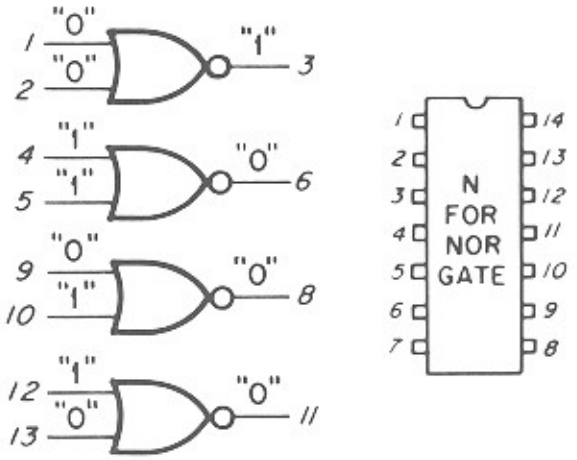
Only 2 NAND gate elements of the 5 input type are packaged into one I.C.



NOR gate

The NOR gate element has 2 inputs and 4 NOR gate elements are packaged into one I.C.

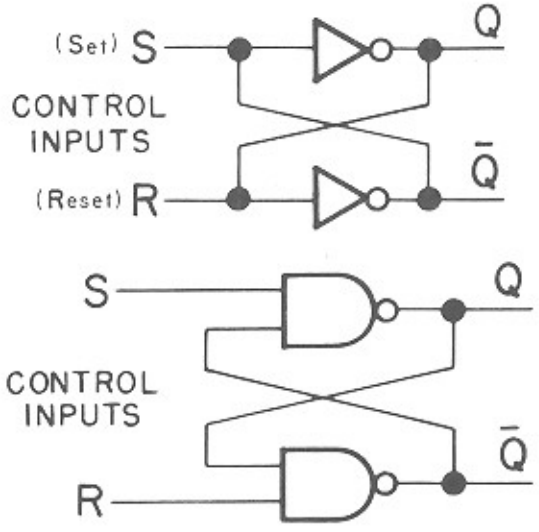
NOR gate Symbol



The output of a NOR gate will be "1" only if all inputs are "O". Any combination of "O" and "1" on the inputs, the output will remain "O".

If the inputs of a NAND or NOR gate are shorted together that gate behaves like a INVERTER.

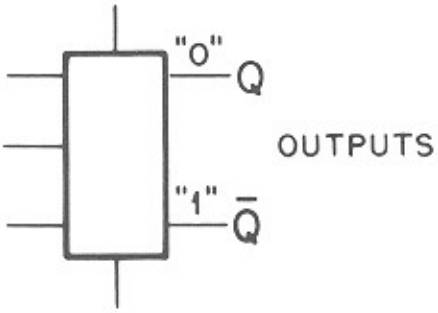
SET/RESET FLIP-FLOP
Memory or Storage Element



This element has two stable states;
Q = "1" and $\bar{Q}$ = "O" or
Q = "O" and $\bar{Q}$ = "1"

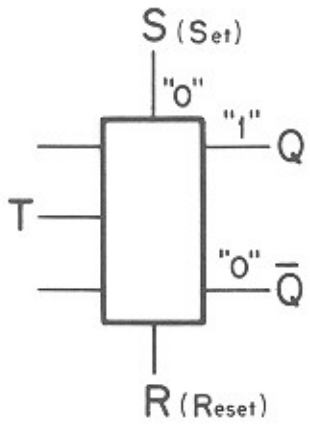
The state of the element can be changed only by application of "O" to one of the control inputs.

FLIP-FLOPS

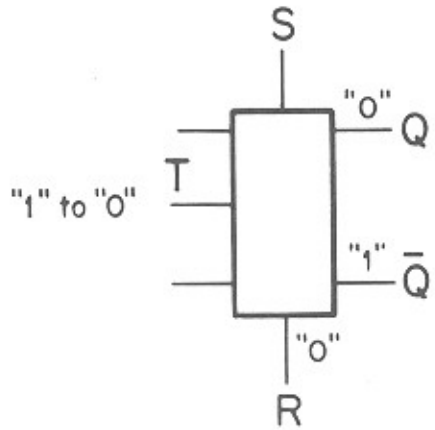


FLIP-FLOP Symbol

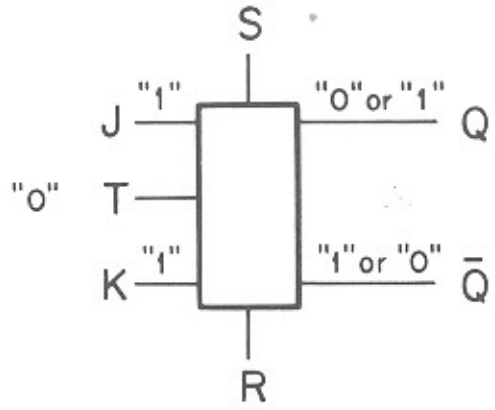
FLIP-FLOP has two outputs, . . . Q and $\bar{Q}$. When one of them is "1" the other is normally "O" and will remain in this condition even after the removal of the signal which caused this condition.



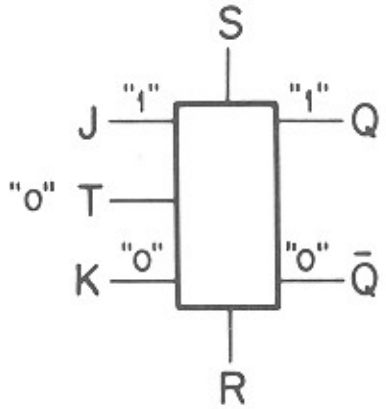
The state of the outputs can be changed by signals on lines S, R and T. A low or "O" on S will make Q high or "1".



$\bar{Q}$ will go high when R is low and a change from high to low on T will switch the outputs to the opposite state. (From high to low or, . . . low to high).

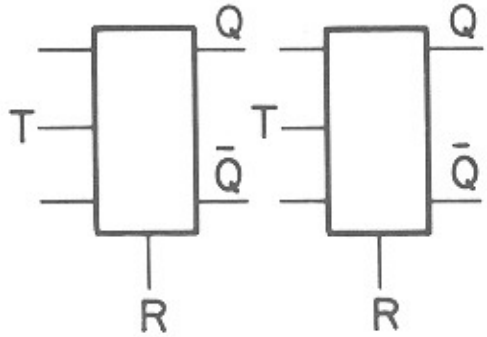


The conditions of J and K inputs control the switching of the outputs by the T input. A high on both J and K will allow the FF to switch for every negative change on T.



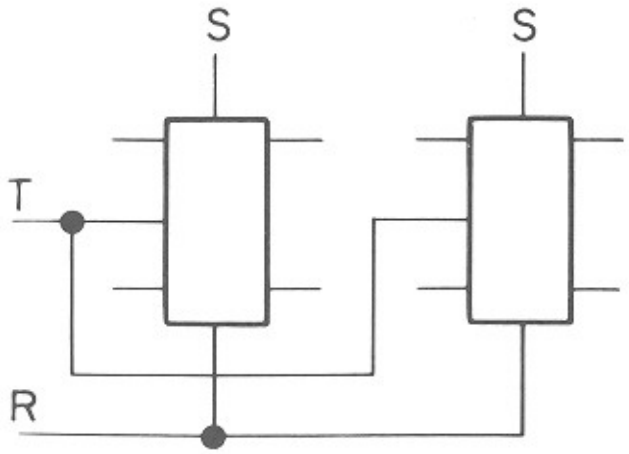
High on J and low on K will allow the FF to switch Q to high. . . . With high on K and low on J, negative change on T will switch $\bar{Q}$ to high.

FLIP-FLOP is used as a memory or storage element and Counter or Divider since the output of FF is half the frequency on input T.



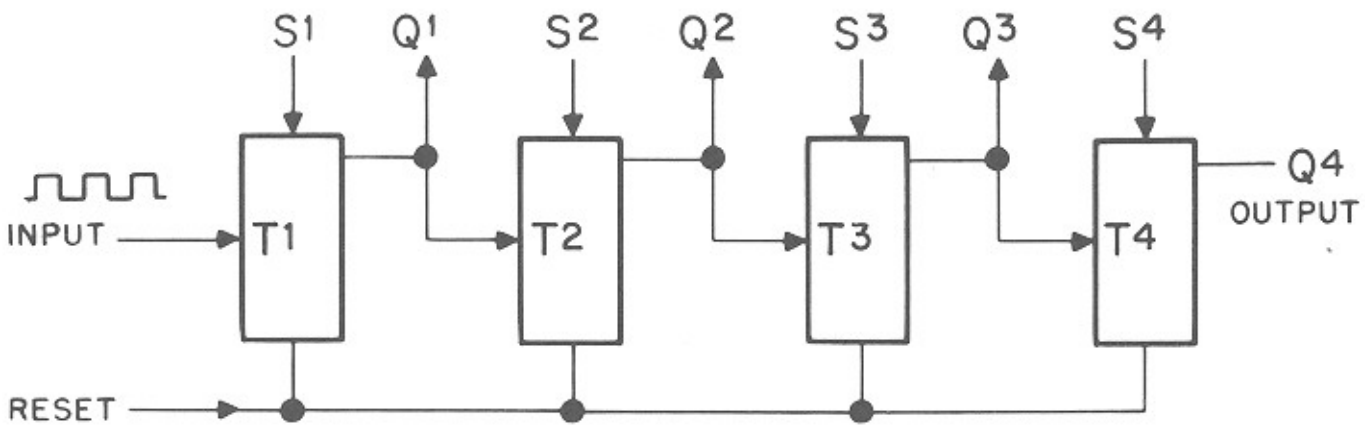
In every I.C. package there are two FF's which may be connected in various manner.

In the Wall Box there are two types of FF I.C.'s; one which has individual R and T inputs and no S lines.



The other has common R and T lines but individual S lines. The two are not interchangeable.

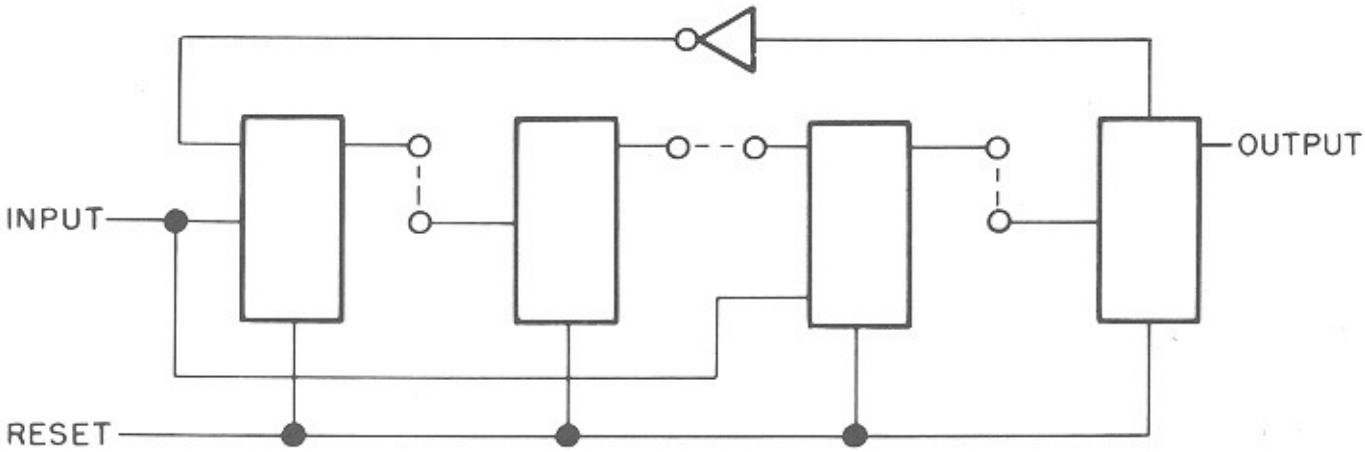
16 BIT COUNTER



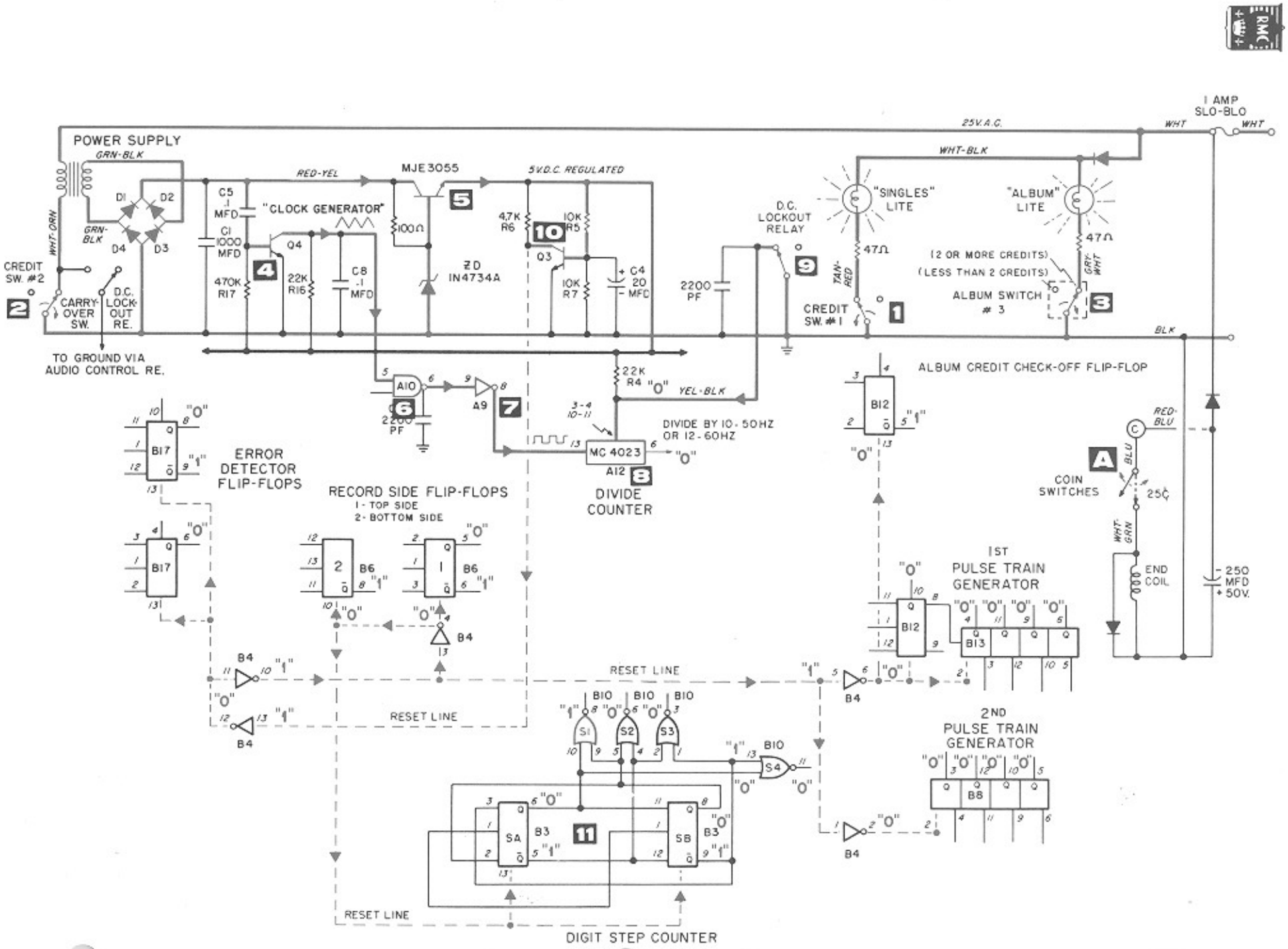
Several FF's connected together as shown make up a "counter". This particular counter is a "divide by sixteen" counter since the output of the last FF is 1/16 of the input.

The states of the outputs 1, 2, 3 and 4 at any time represent a "count or a "number" of which there are 16 possible. This count can be preset by making the proper S lines low. This counter can also be "cleared" that is, all outputs made low by making Reset Line low.

UNIVERSAL COUNTER



The Universal Counter operates in the same fashion as the straight counter with the exception that there are provisions for various interconnections of the individual FF's by which the count can be varied. The connections shown on the diagram are for divide by 10 counter, or the output is 1/10 of the input.


POWER SUPPLY
GRN-BLK
WHT-ORN
GRN-BLK
D1
D2
D3
D4
C5 .1 MFD
C1 1000 MFD
"CLOCK GENERATOR"
RED-YEL
MJE3055
5 V.D.C. REGULATED
100Ω
ZD IN4734A
4.7K R6
10K R5
Q3
10K R7
C4 20 MFD
2200 PF
470K R17
Q4
22K R16
C8 .1 MFD
CREDIT SW. #2
CARRY-OVER SW.
D.C. LOCK-OUT RE.
TO GROUND VIA AUDIO CONTROL RE.
25 V.A.C.
WHT
WHT
1 AMP SLO-BLO
WHT-BLK
D.C. LOCKOUT RELAY
"SINGLES" LITE
"ALBUM" LITE
47Ω
47Ω
TAN-RED
GRY-WHT
(2 OR MORE CREDITS)
(LESS THAN 2 CREDITS)
ALBUM SWITCH # 3
CREDIT SW. #1
BLK
22K R4
YEL-BLK
A10
A9
2200 PF
3-4
10-11
DIVIDE BY 10 - 50HZ OR 12 - 60HZ
MC 4023
A12
DIVIDE COUNTER
ALBUM CREDIT CHECK-OFF FLIP-FLOP
B12
RED-BLU
BLU
COIN SWITCHES
25¢
WHT
GRN
END COIL
250 MFD + 50V.
ERROR DETECTOR FLIP-FLOPS
B17
RECORD SIDE FLIP-FLOPS
1 - TOP SIDE
2 - BOTTOM SIDE
B6
B4
1ST PULSE TRAIN GENERATOR
B13
RESET LINE
B10
S1
S2
S3
S4
2ND PULSE TRAIN GENERATOR
B8
S A
S B
B3
DIGIT STEP COUNTER

SEQUENCE No. 1
25c COIN DROPPED

At standby, power supply is disconnected to the logic circuits.

Insertion of a 25¢ coin pulses the respective Coin Switch (A). . . . Master Ratchet escapes two teeth . . . Two credits register.

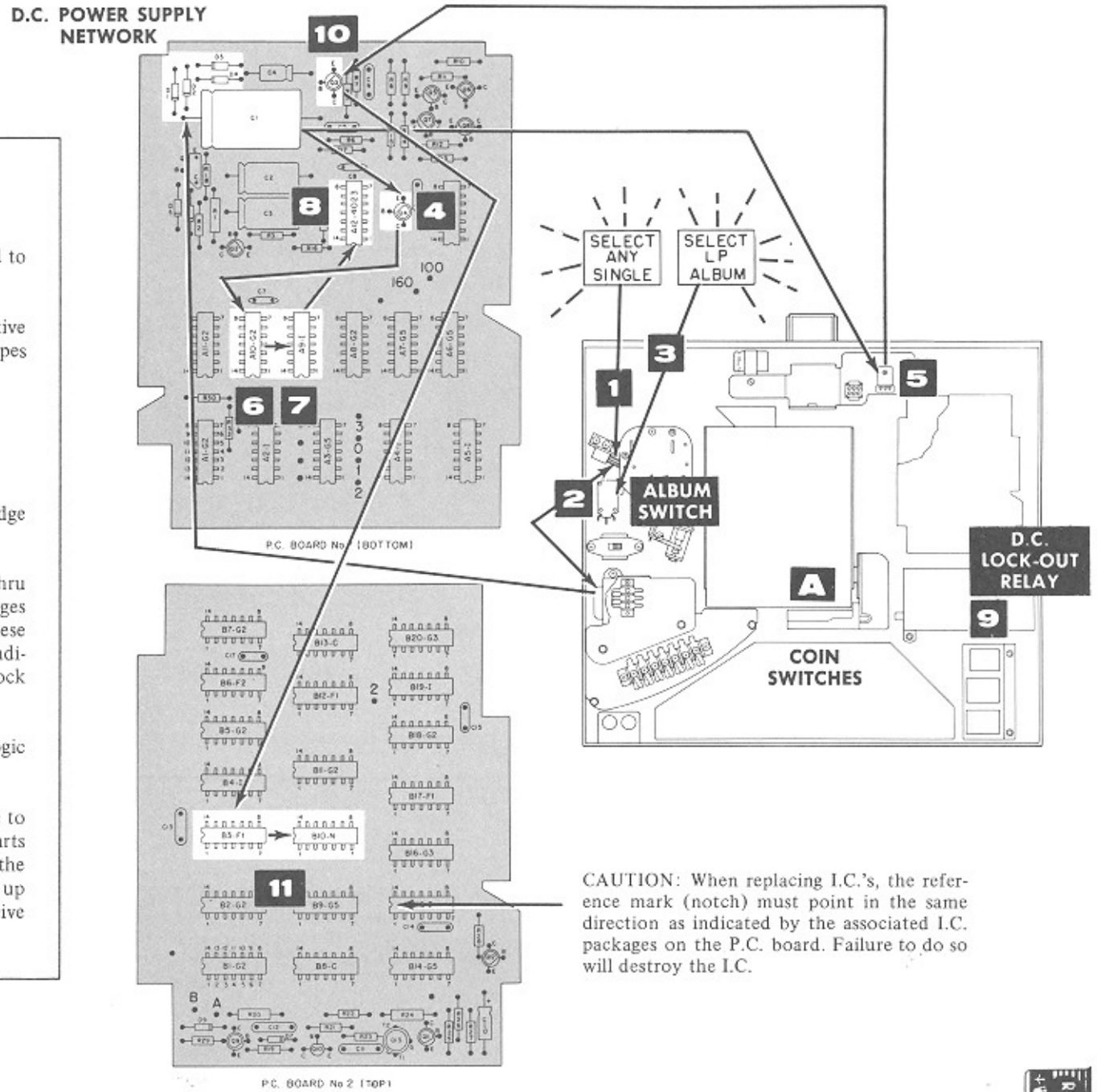
(1) Lites the "Singles" Select Lite.
(2) Turns on the D.C. Power Supply.
(3) Lites the "Album" lite.

The unfiltered D.C. current from the bridge rectifier activates Transistors (4) & (5).

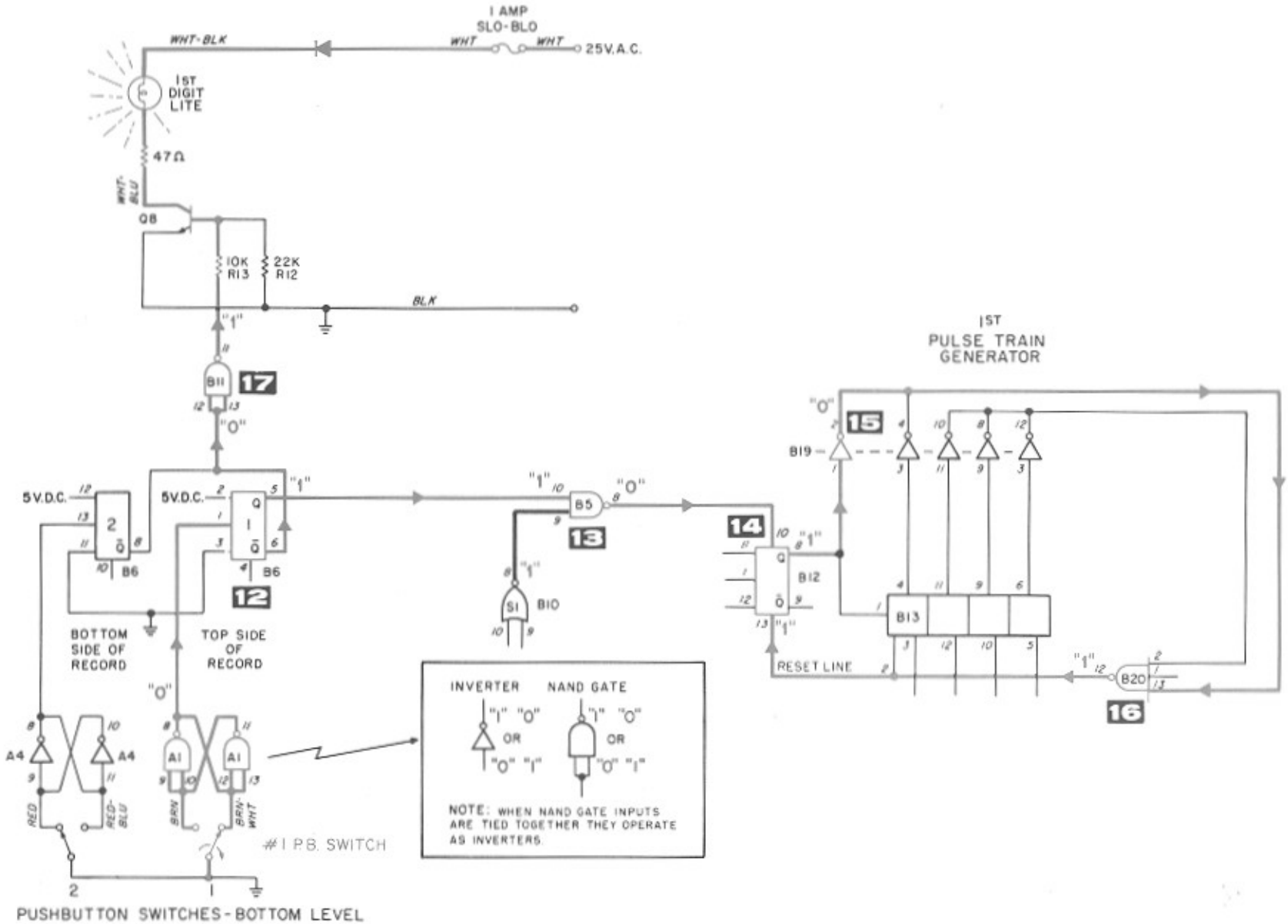
Output of Transistor (4), after passing thru NAND gate (6) and INVERTER (7), changes the ripple oscillations to square pulses. These pulses are then "clamped" to a "hold" condition in the Divide Counter (8) via D.C. Lock Out relay switch (9).

Transistor (5) regulates 5 V.D.C. to the logic system and turns on Transistor (10).

Transistor (10) supplies a "1" (high) pulse to the logic circuits to insure that the system starts from a standby or zero condition. . . . At the same time, Digit Step Counter (11) sets up NOR gate "S1" output to a "1" state to receive the 1st Digit number.



CAUTION: When replacing I.C.'s, the reference mark (notch) must point in the same direction as indicated by the associated I.C. packages on the P.C. board. Failure to do so will destroy the I.C.


1 AMP
SLO-BLO
WHT-BLK
WHT
WHT
25V.A.C.
1ST
DIGIT
LITE
47Ω
WHT-BLU
Q8
10K
R13
22K
R12
BLK
"1"
B11
17
12
13
"0"
5V.D.C.
5V.D.C.
"1"
B6
B6
12
BOTTOM
SIDE OF
RECORD
TOP SIDE
OF
RECORD
"0"
"1"
10
B5
"0"
13
"1"
S1
B10
1ST
PULSE TRAIN
GENERATOR
"0"
15
B19
14
"1"
B12
"1"
B13
RESET LINE
"1"
B20
16
A4
A4
A1
A1
RED
RED-BLU
BRN
BRN-WHT
#1 P.B. SWITCH
2
1
PUSHBUTTON SWITCHES - BOTTOM LEVEL
INVERTER
NAND GATE
"1" "0"
OR
"0" "1"
"1" "0"
OR
"0" "1"
NOTE: WHEN NAND GATE INPUTS
ARE TIED TOGETHER THEY OPERATE
AS INVERTERS.

SEQUENCE No. 2
1st DIGIT NUMBER PRESSED

The 1st Digit number relates to the record side.

No. 1 Pushbutton selects "top side" of record selection, . . . No. 2, the "bottom side".

Incorrect Digit numbers, or two or more P.B. switches pressed at the same time result in a "no go" condition and causes the "Reset and Reselect" lamp to lite.

Reset Button must be pressed to clear the system before re-selecting. This circuit is explained later.

Upon pressing P.B. switch, as #1, the Digit number must be validated and stored in the 1st Pulse Train Generator.

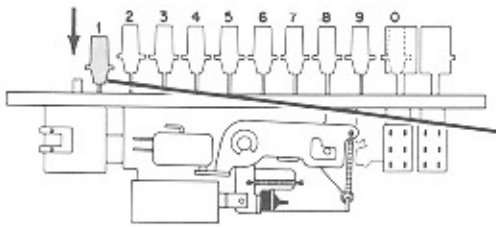
The "down" position of the P.B. switch changes the output of the dual NAND gates to a "O" state causing FLIP-FLOP (12) to trigger. After the trigger, Q output is driven "1", . . . the $\bar{Q}$ to "O".

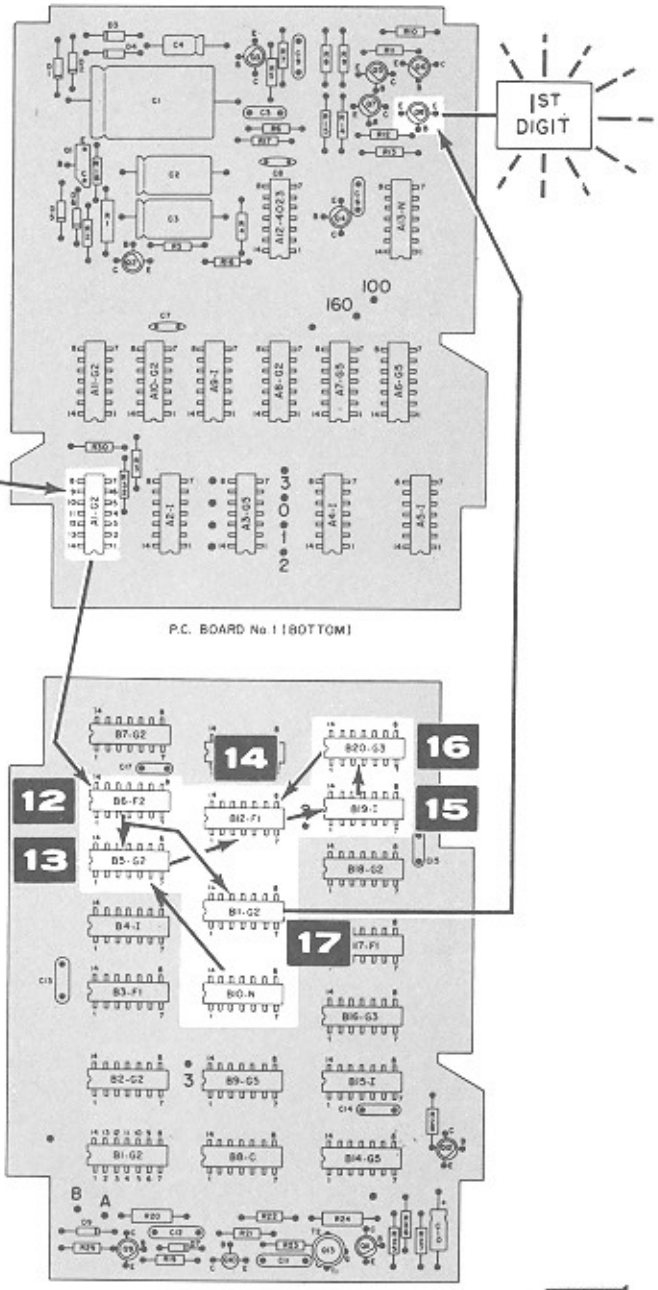
The "1" state of Q is applied to one input of NAND gate (13). Since the 2nd input of NAND gate (13) is set to a "1" state, (supplied from the output of NOR gate "S1"), the output changes to "O" and sets the Q output of FLIP-FLOP (14) to "1". This code is then stored by shifting the Reset Line to a "1" state via INVERTER (15) and NAND gate (16).

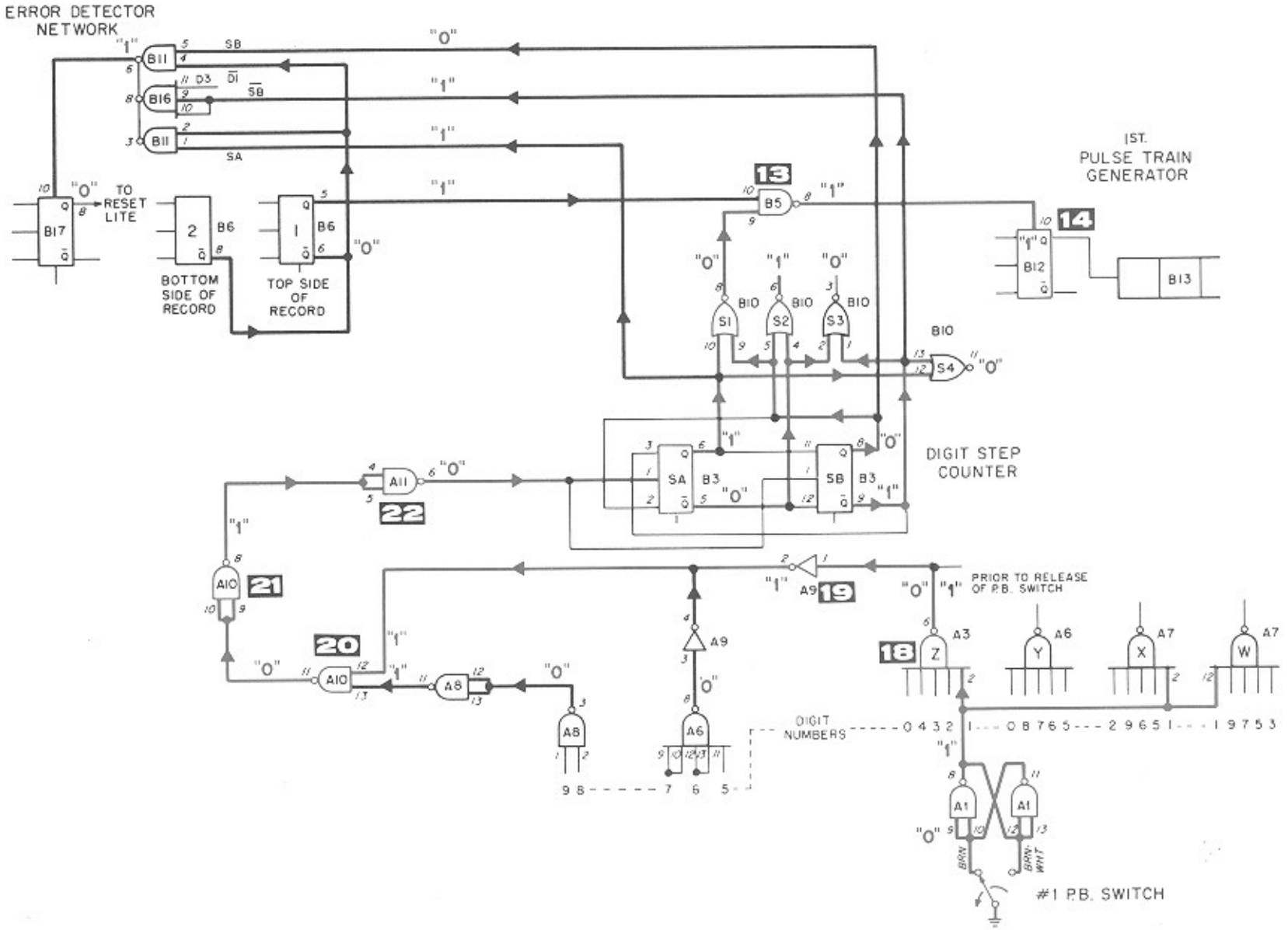
Note: In the case of P.B. switch #2 being pressed for the 1st Digit number, FLIP-FLOP (14) in the 1st Pulse Train Generator is not activated and remains in a "O" state. This "O" signal represents the code to play the "bottom side" of the record.

The 1st Pulse Train Generator Reset Line also remains in a "O" state until the 2nd Digit number is pressed.

The $\bar{Q}$ "O" output of NAND gate (12), after passing thru NAND gate (17), changes to a "1" state which drives the Transistor in the circuit to turn on the 1st Digit lite.






ERROR DETECTOR NETWORK
"1"
B11
SB
"0"
B16
SB
"1"
B11
SA
"1"
"1"
"0"
TO RESET LITE
B17
2
B6
BOTTOM SIDE OF RECORD
1
B6
TOP SIDE OF RECORD
"0"
13
B5
"1"
"0"
"1"
"0"
S1
S2
S3
B10
S4
"0"
1ST. PULSE TRAIN GENERATOR
14
"1"
B12
B13
DIGIT STEP COUNTER
SA
B3
SB
B3
"1"
"0"
"1"
"0"
22
A11
"0"
"1"
21
A10
20
"1"
"0"
A10
"1"
A8
"0"
A8
A9
19
"1"
A9
"0"
"1"
PRIOR TO RELEASE OF P.B. SWITCH
18
Z
A3
Y
A6
X
A7
W
A7
DIGIT NUMBERS
0 4 3 2 - - - 0 8 7 6 5 - - - 2 9 6 5 1 - - - 1 9 7 5 3
9 8 - - - - - 7 6 5 - -
A6
"0"
"1"
A1
A1
"0"
BRN
BRN-WHT
#1 P.B. SWITCH

SEQUENCE No. 3
1st DIGIT NUMBER RETURNS

Prior to the release of the #1 P.B. switch, the output of NAND gate (18) is in a "1" state. This signal, after passing thru INVERTER (19) and NAND gates (20), (21) & (22), is a logical "1" at the Digit Step Counter.

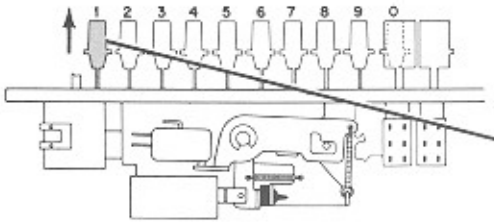
When the 1st Digit P.B. switch returns, the output signal of the dual NAND gates changes to "1". Since all P.B. switches are "up", the "O" signal from the output of NAND gate (18) advances thru the INVERTER (19) and NAND gates (20), (21) & (22). The input line to the Digit Step Counter changes from "1" to "O". This change causes FLIP-FLOP "SA" to toggle setting the Q output to "1" and $\bar{Q}$ to "O".

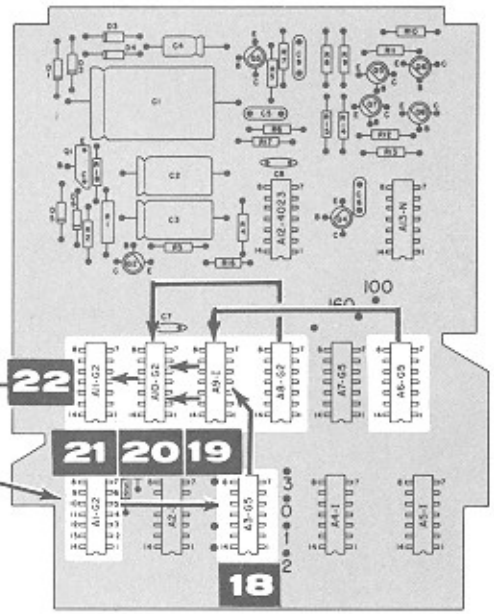
The combination of "SA" and "SB" outputs are applied to the 4 NOR gates in the network. This results in transferring the "1" state output from "S1" to "S2" NOR gate.

The "O" output state of "S1" now changes the output of NAND gate (13) from "O" to "1". This high signal locks-up the 1st Digit record side information in FLIP-FLOP (14) section of the 1st Pulse Train Generator.

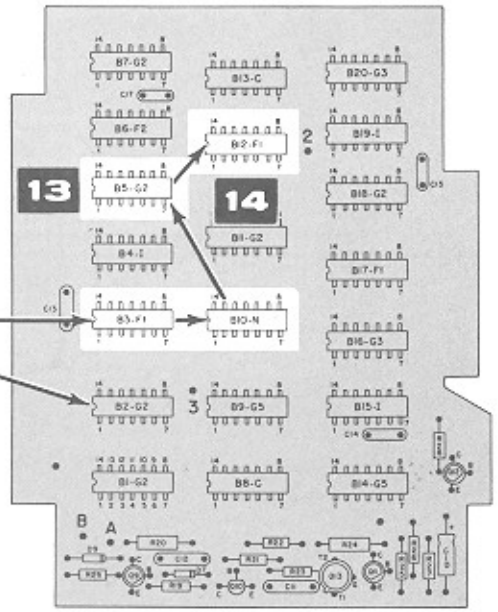
Since the Error Detector Network noted no malfunctions, the output line of the 3 NAND gates remains clamped to a "1" state (no errors), system condition are "go".

The "1" state output of "S2" is the ready signal to accept the 2nd Digit number.



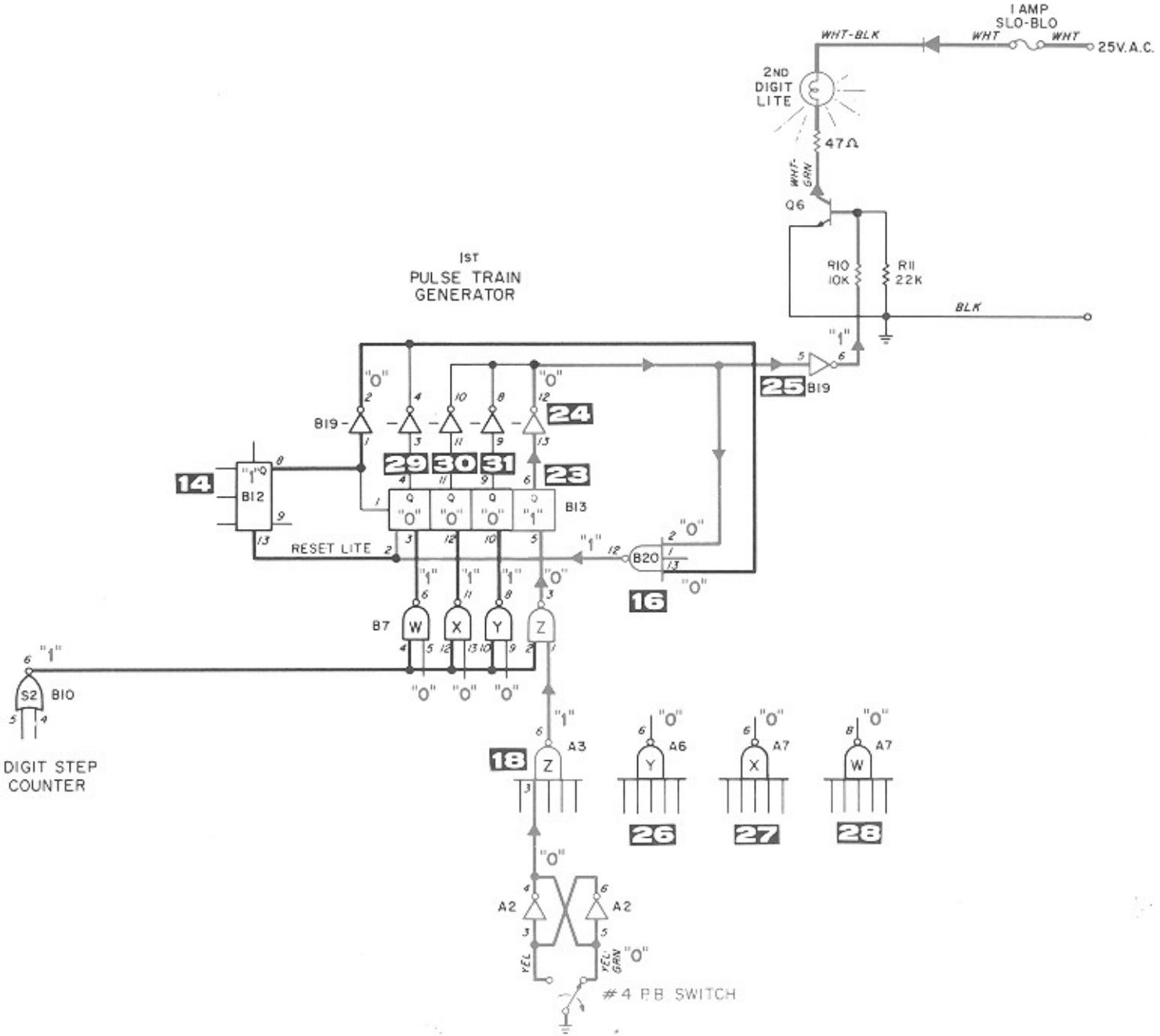


P.C. BOARD No.1 (BOTTOM)



P.C. BOARD No.2 (TOP)

CAUTION: When replacing I.C.'s, the reference mark (notch) must point in the same direction as indicated by the associated I.C. packages on the P.C. board. Failure to do so will destroy the I.C.


1 AMP
SLO-BLO
WHT-BLK
WHT
WHT
25V.A.C.
2ND
DIGIT
LITE
47Ω
WHT-GRN
Q6
R10
10K
R11
22K
BLK
1ST
PULSE TRAIN
GENERATOR
"1"
"0"
25 B19
24
B19
29 30 31
23
14
B12
B13
RESET LITE
B20
16
B7
W
X
Y
Z
S2
B10
DIGIT STEP
COUNTER
18
A3
26
A6
27
A7
28
A7
A2
A2
YEL
YEL GRN
#4 P.B. SWITCH

SEQUENCE No. 4
2nd DIGIT NUMBER PRESSED

The state of the system at this interval is as follows:

(A) Digit Step Counter advanced 1 count.
(B) Output of "S2" NOR gate now in a "1" state and applied to 1 input of NAND gates (W), (X), (Y) & (Z) in the 1st Pulse Train Generator.

2nd Digit #4 pressed. . . . The "down position of the P.B. switch changes the dual INVERTER output to "O" which raises the output signal of NAND gate (18) to "1".

The "1" state line is applied to the 2nd input of NAND gate (Z). Both inputs now "1", drives the output to "O" which sets the Q output of FLIP-FLOP (23) to "1" where it is stored by the "1" state condition of the Reset Line.

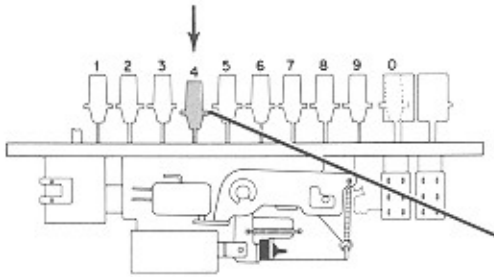
The "O" output of INVERTER (24), after passing thru INVERTER (25), changes to "1". The high signal turns on the Transistor in the circuit causing the 2nd Digit lamp to lite.

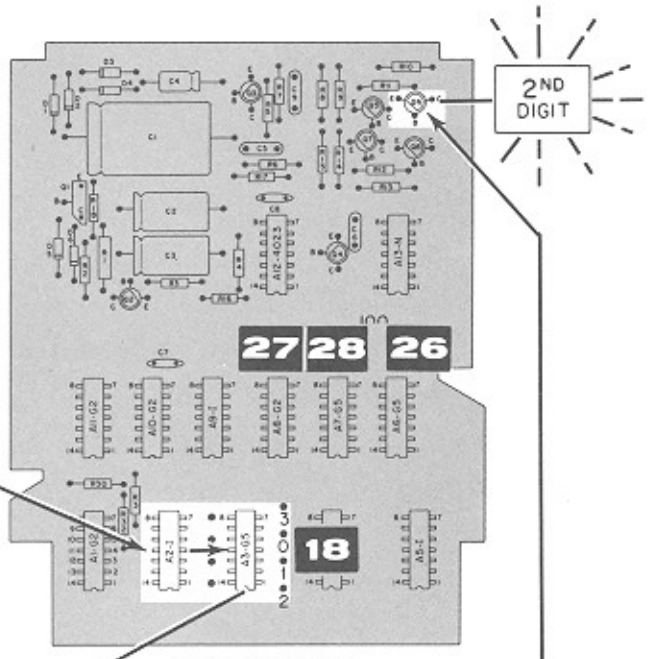
Since NAND gates (26), (27) & (28) are not activated for P.B. switch #4, the Q outputs of FLIP-FLOP (29), (30) & (31) in the 1st Pulse Train Generator remain in a "O" state.

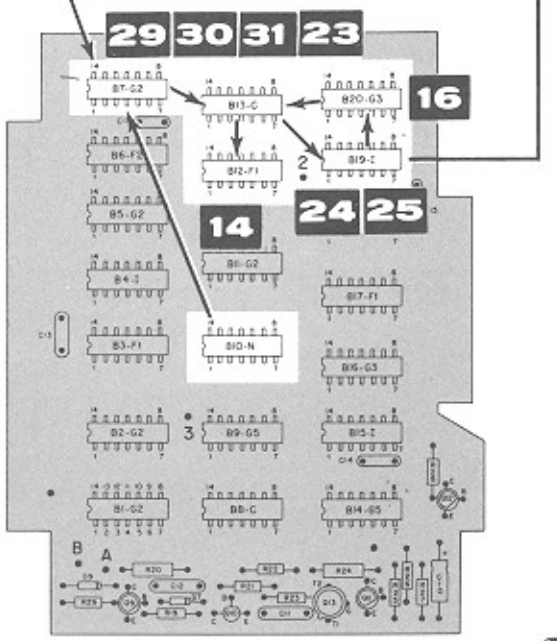
The output condition of the 1st Pulse Train Generator is as follows:

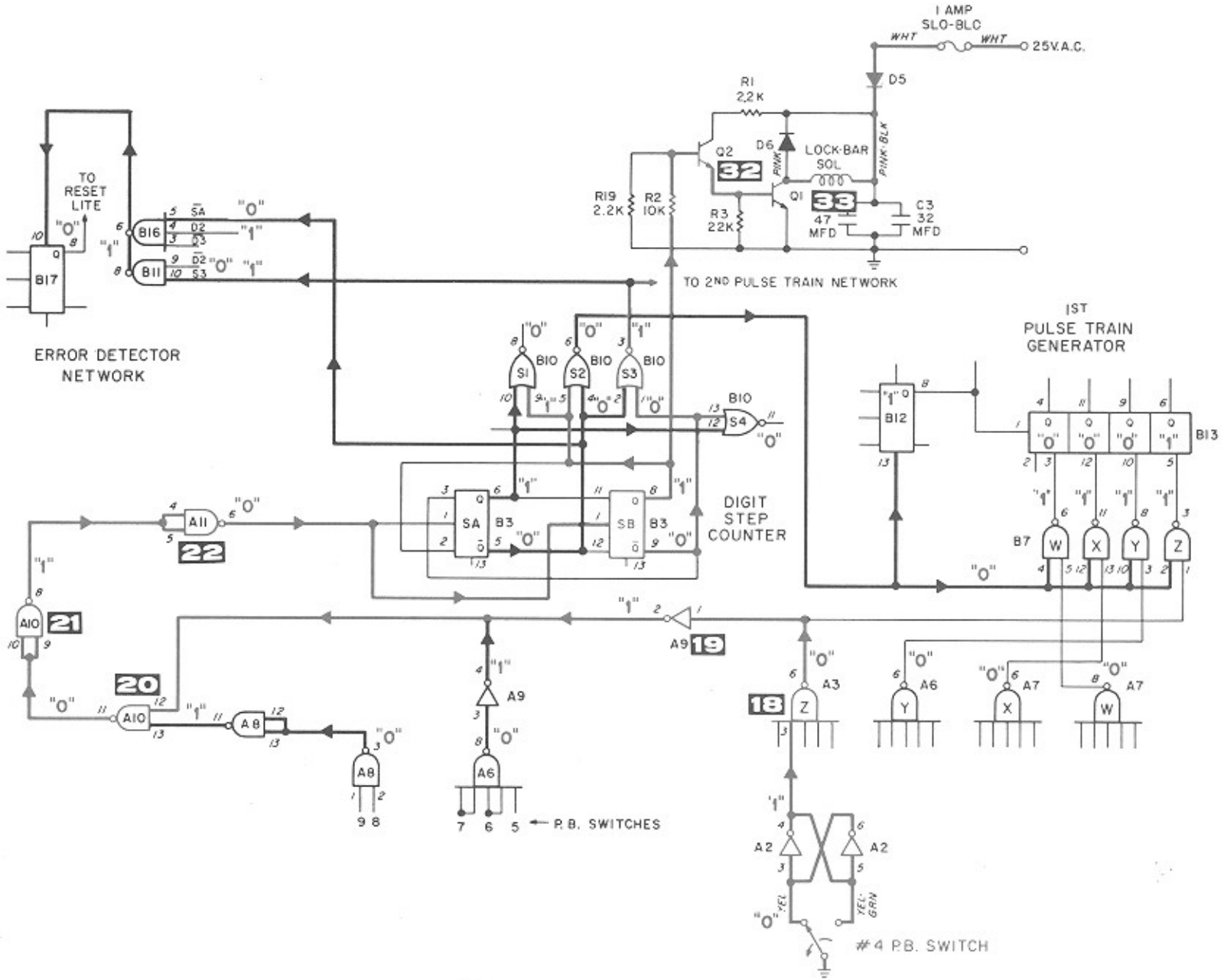
FLIP-FLOP (23) – "1"
(31) – "0"
(30) – "0"
(29) – "0"
(14) – "1" (Stored by the 1st Digit number)

The "code" for the 1st Pulse Train is now stored by the "1" state of the reset line and no further action takes place until the P.B. switch returns.








1 AMP
SLO-BLO
WHT
WHT
25V.A.C.
D5
R1
2.2K
Q2
32
D6
PINK
LOCK-BAR
SOL
PINK-BLK
Q1
33
R19
2.2K
R2
10K
R3
22K
47
MFD
C3
32
MFD
TO 2ND PULSE TRAIN NETWORK
TO
RESET
LITE
ERROR DETECTOR
NETWORK
B16
B11
B17
1ST
PULSE TRAIN
GENERATOR
B12
B13
B7
W
X
Y
Z
S1
S2
S3
S4
BIO
SA
SB
B3
DIGIT
STEP
COUNTER
A11
22
A10
21
20
A8
A9
19
18
A3
A6
A7
A2
P.B. SWITCHES
#4 P.B. SWITCH
YEL
GRN

SEQUENCE No. 5
2nd DIGIT NUMBER RETURNS

When #4 P.B. switch is released, the "up" position changes the dual INVERTER output to a "1" state and applied to 1 input of NAND gate (18). . . . Since all P.B. switches are "up", the "O" output state of NAND gate (18) repeats the signal transmission thru INVERTER (19) and NAND gates (20), (21) and (22) as explained in Sequence No. 3 for validating the 1st Digit number.

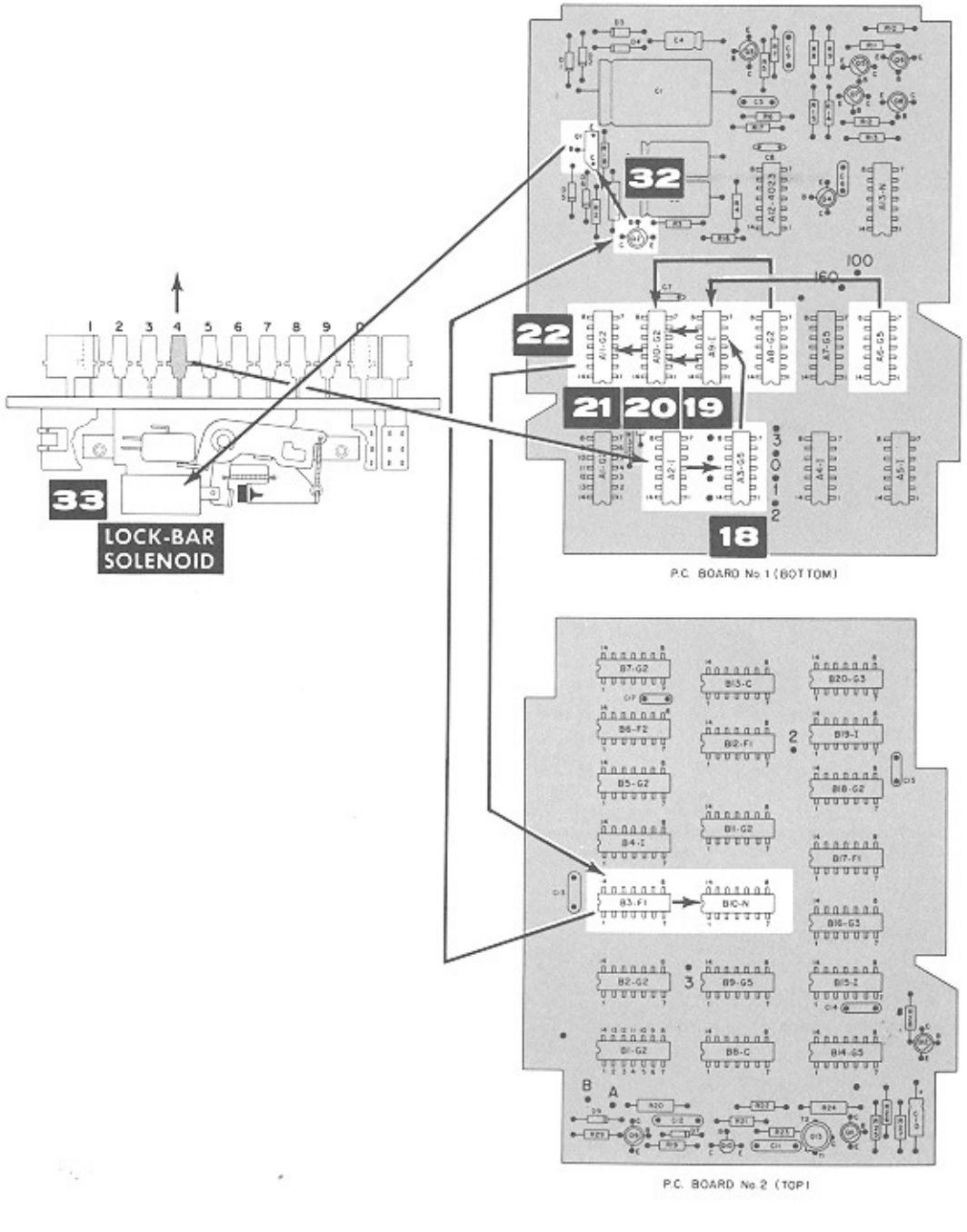
The change of the output state of NAND gate (22) activates the Digit Step Counter causing the Q output of FLIP-FLOP "SB" to change state from "O" to "1" which turns on 2 Transistors (32). . . . Lock Bar Solenoid (33) energizes to "hold" the 3rd Digit number when pressed. The $\bar{Q}$ output of FLIP-FLOP "SB" changes from "1" to "O".

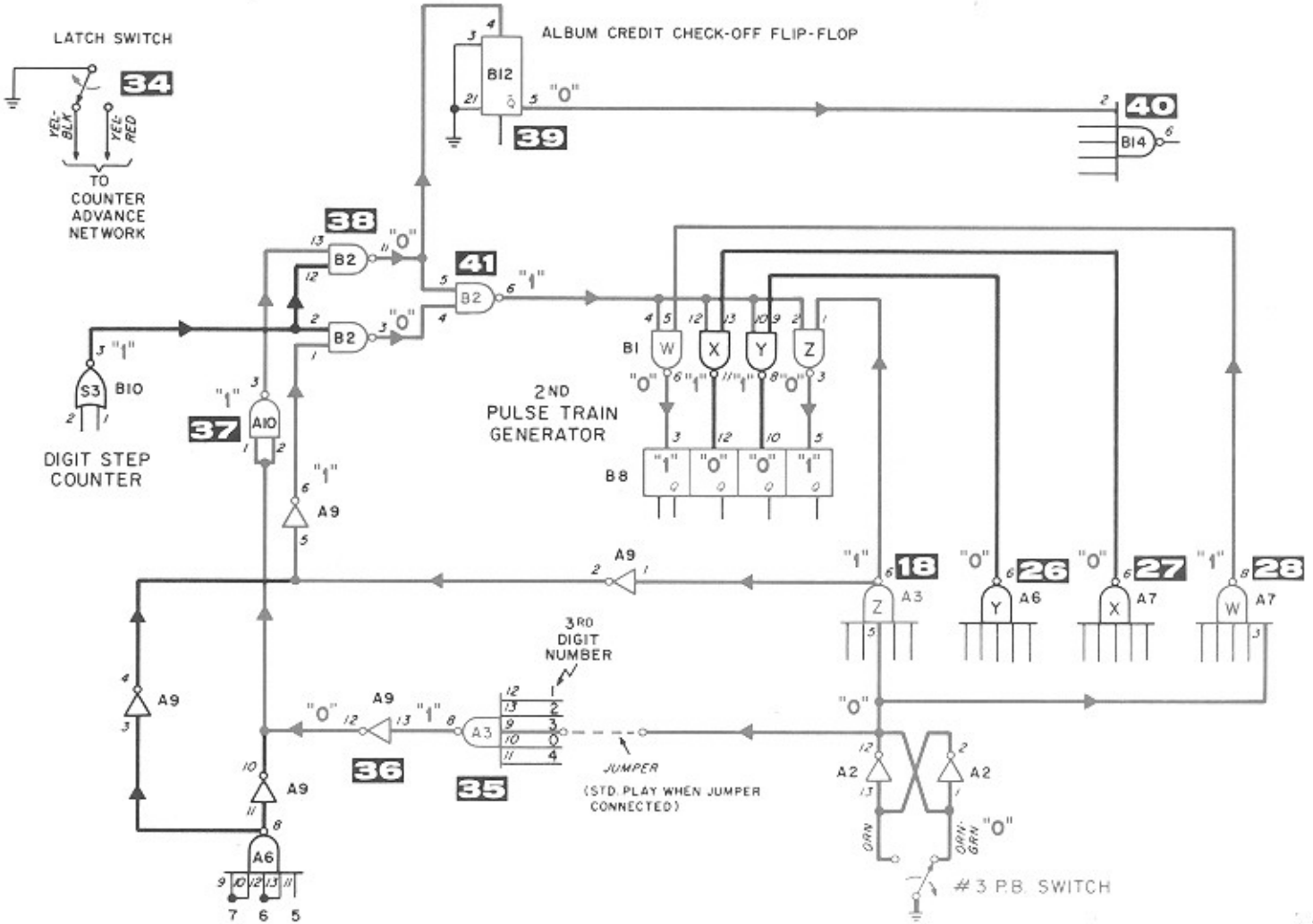
The new combination of the 4 output signal levels at "SA" and "SB" advance the "1" output state from NOR gate "S2" to NOR gate "S3".

The "O" output of NOR gate "S2" is applied to NAND gates (W), (X), (Y) & (Z), and the resultant "1" state outputs lock-up the stored 1-0-0-0-1 code in the 1st Pulse Train Generator.

Since no system malfunctions were noted by the Error Detector Network during the transmission of the 2nd Digit number, the "1" state output of NOR gate "S3" is now applied to the 2nd Pulse Train network.

The system is now ready to accept the 3rd Digit number.




LATCH SWITCH
34
YEL-BLK
YEL-RED
TO COUNTER ADVANCE NETWORK
ALBUM CREDIT CHECK-OFF FLIP-FLOP
B12
"0"
39
40
B14
38
B2
"0"
41
"1"
B2
B2
"0"
"1"
S3
B10
DIGIT STEP COUNTER
37
A10
"1"
A9
2ND PULSE TRAIN GENERATOR
B1
W
X
Y
Z
"0" "1" "1" "0"
B8
"1" "0" "0" "1"
A9
"1"
18
A3
"0"
26
A6
"0"
27
A7
"1"
28
A7
3RD DIGIT NUMBER
A9
"0"
A9
"1"
A3
36
35
JUMPER
(STD. PLAY WHEN JUMPER CONNECTED)
"0"
A2
A2
GRN
ORN-GRN
"0"
#3 P.B. SWITCH
A9
A9
A6
7 6 5

SEQUENCE No. 6
3rd DIGIT NUMBER PRESSED

When the 3rd Digit number is pressed, as #3, the P.B. switch is "held" by the energized Lock Bar Solenoid. P.B. Latch switch (34) transfers after a short mechanical delay.

The 3rd Digit data is stored during the short interval of the down stroke of the P.B. switch and the transfer of the Latch switch.

The "down" position of the P.B. switch changes the dual INVERTER output to "O". The "O" line is applied to one input of NAND gates (35), (28) & (18) changing the NAND gate outputs to "1".

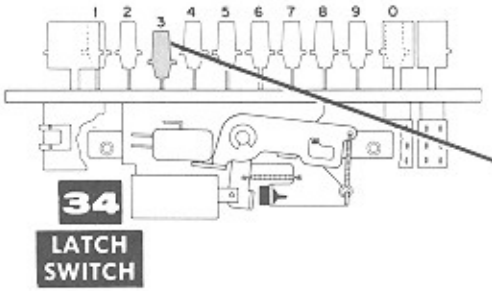
NAND gate (35) provides for the removal of one credit for a "Singles" selection. (Album programming and credit removal is explained later.)

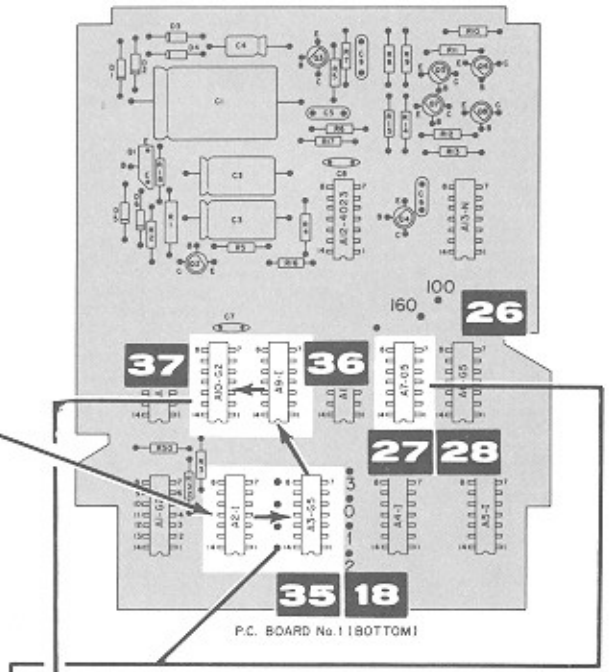
The high output signal of NAND gate (35) after making "O" "1" transitions thru INVERTER (36) and NAND gate (37), becomes "O" at the output of NAND gate (38). This sets the $\overline{Q}$ output of FLIP-FLOP (39) to "O" which is applied to one input of NAND gate (40). The NAND gate now remains inactive for a "Singles" selection.

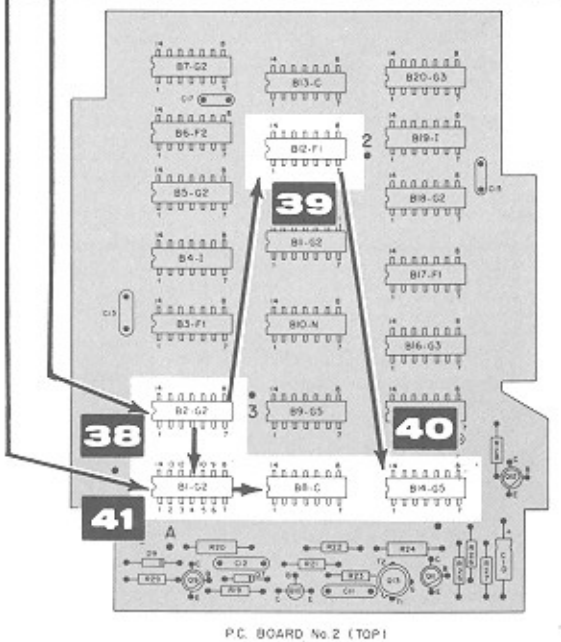
The "1" state output of NAND gate (41) is clamped to one input of NAND gates (W), (X), (Y) & (Z) in the 2nd Pulse Train Generator. The 2nd input signal is provided by NAND gates (18), (26), (27) & (28). This results in switching the outputs of NAND gates (W) & (Z) to "O" which stores a "1" state at the Q outputs of their respective FLIP-FLOPS. . . .

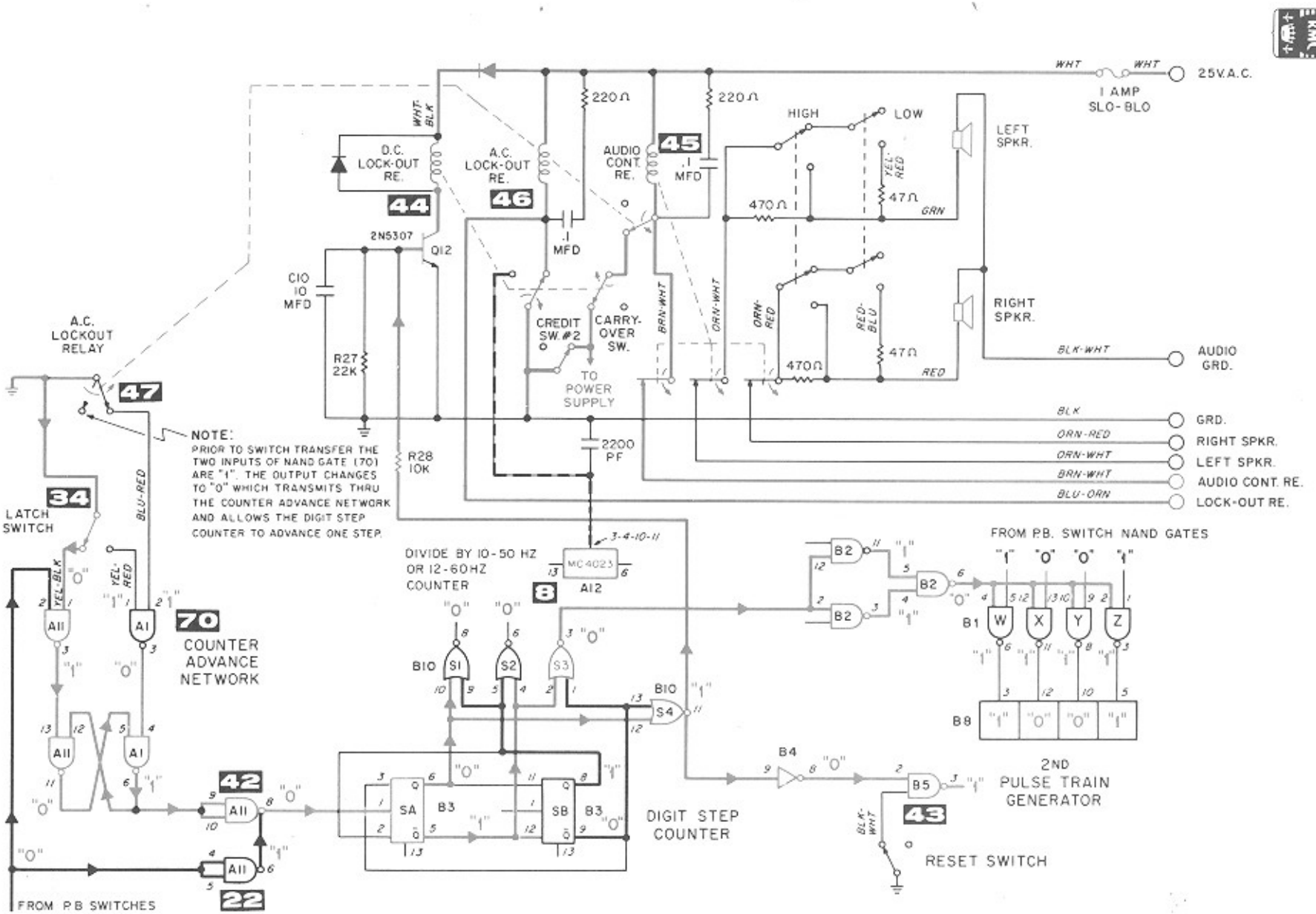
Since the outputs of NAND gates (X) & (Y) remain in a "1" state, their respective FLIP-FLOPS remain in a "O" state.

The code of 1-0-0-1 is now stored in the 2nd Pulse Train Generator. Digit Step Counter now must advance one step to lock-up the stored code and start transmission to the Receiver.








WHT
WHT
25V.A.C.
1 AMP
SLO-BLO
220Ω
220Ω
WHT-BLK
D.C. LOCK-OUT RE.
A.C. LOCK-OUT RE.
AUDIO CONT. RE.
45
.1 MFD
HIGH
LOW
LEFT SPKR.
YEL-RED
47Ω
GRN
470Ω
44
46
2N5307
Q12
.1 MFD
C10 10 MFD
ORN-RED
RED-BLU
47Ω
RED
470Ω
RIGHT SPKR.
BLK-WHT
AUDIO GRD.
CREDIT SW. #2
CARRY-OVER SW.
BRN-WHT
ORN-WHT
TO POWER SUPPLY
A.C. LOCKOUT RELAY
47
R27 22K
BLK
GRD.
ORN-RED
RIGHT SPKR.
ORN-WHT
LEFT SPKR.
BRN-WHT
AUDIO CONT. RE.
BLU-ORN
LOCK-OUT RE.
2200 PF
R28 10K
NOTE:
PRIOR TO SWITCH TRANSFER THE TWO INPUTS OF NAND GATE (70) ARE "1". THE OUTPUT CHANGES TO "0" WHICH TRANSMITS THRU THE COUNTER ADVANCE NETWORK AND ALLOWS THE DIGIT STEP COUNTER TO ADVANCE ONE STEP.
34
LATCH SWITCH
BLU-RED
YEL-BLK
YEL-RED
DIVIDE BY 10-50 HZ OR 12-60HZ COUNTER
3-4-10-11
MC4023
A12
8
FROM P.B. SWITCH NAND GATES
"1" "0" "0" "1"
B1
W
X
Y
Z
B8
"1" "0" "0" "1"
70
COUNTER ADVANCE NETWORK
BIO
S1
S2
S3
S4
B4
B5
2ND PULSE TRAIN GENERATOR
42
SA
SB
B3
DIGIT STEP COUNTER
43
RESET SWITCH
BLK-WHT
22
FROM P.B SWITCHES

SEQUENCE No. 7
DIGIT STEP COUNTER ADVANCES— STORED CODE IN THE 2nd PULSE TRAIN GENERATOR LOCKED UP

Since the 3rd Digit P.B. switch is "held" by the energized Lock Bar Solenoid, a "1" state is clamped at the output of NAND gate (22) preventing the Digit Step Counter from advancing one count. The "1" state must be shifted to "O" which is the function of the P.B. Latch switch (34).

As stated before, the 3rd Digit data is stored during the interval of the P.B. switch down stroke and transfer of the the Latch switch.

Latch Switch (34) now transferred to its new position transmits a low signal thru the NAND gate stages in the Counter Advance Network. Upon completion of the "O" and "1" transitions, the output of the last NAND gate (42) in the network is driven "O".

The "O" state output activates the Digit Step Counter causing FLIP-FLOP "SA" to reset the Q output to "O" and $\overline{Q}$ to "1". This results in transferring the "1" state output of NOR gate "S3" to NOR gate "S4".

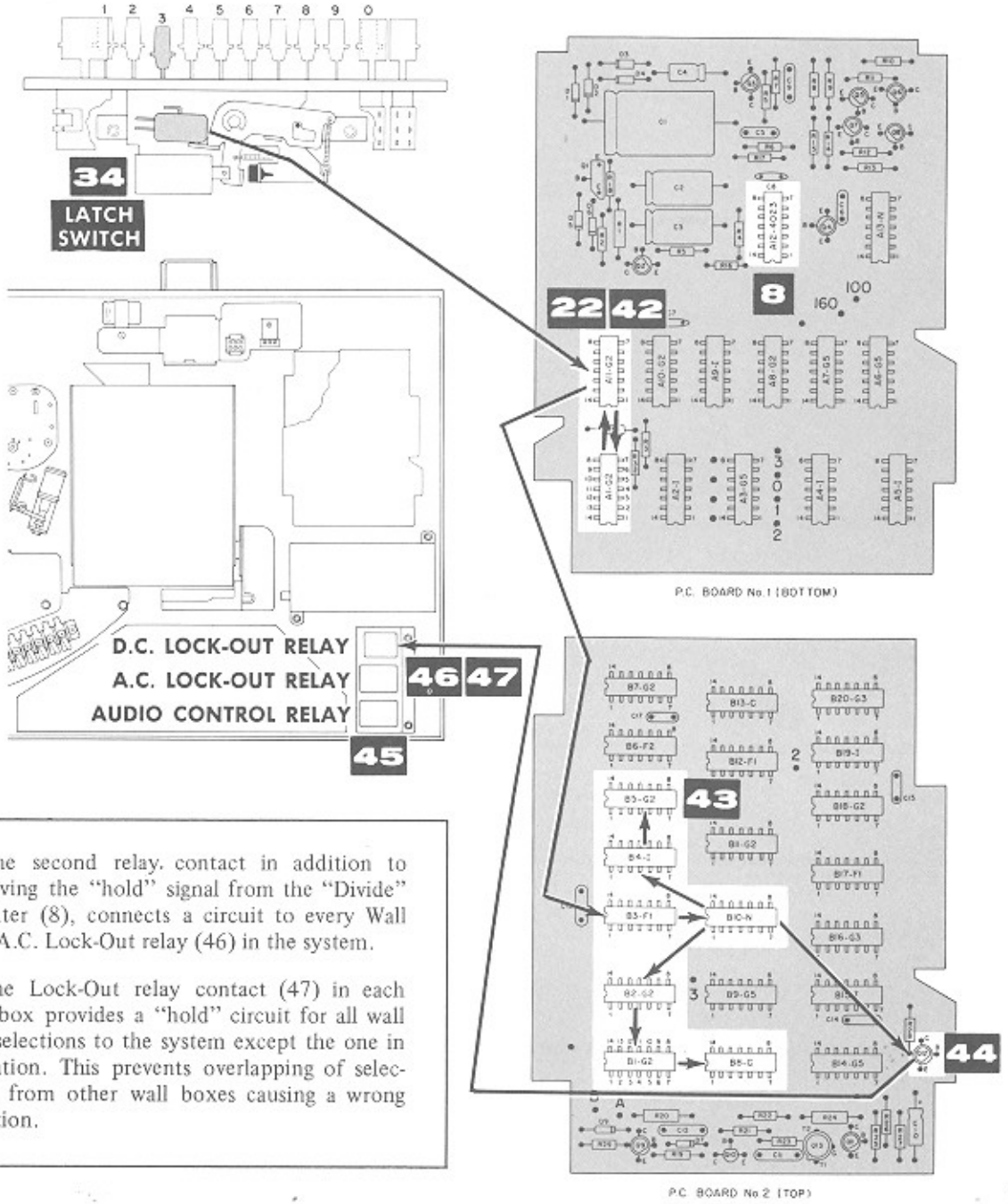
The "O" output signal of "S3" locks-up the stored code in the 2nd Pulse Train Generator.

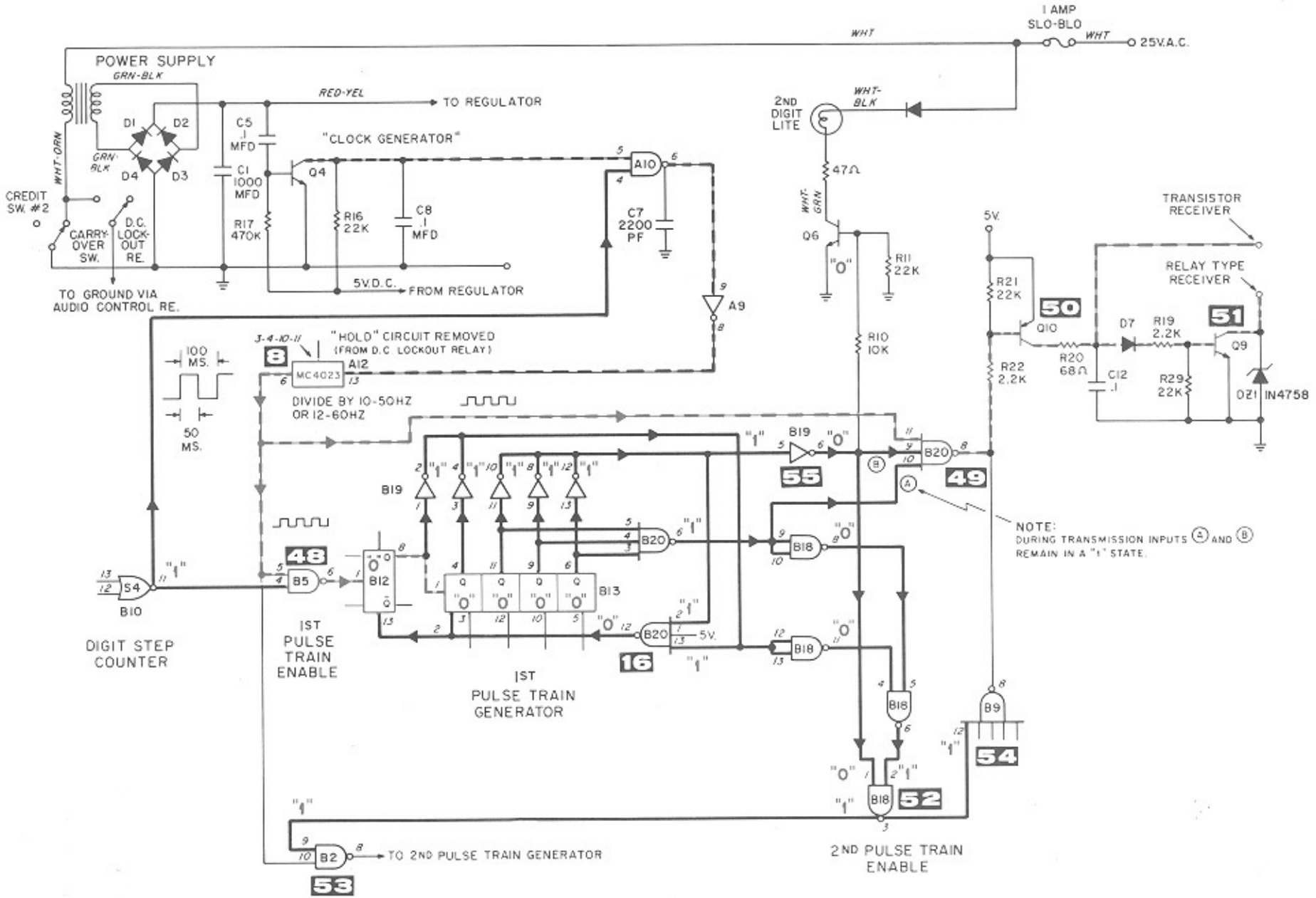
The "1" output signal of "S4" disables the Reset button NAND gate (43) in addition to energizing the D.C. Lock-Out relay after a short time delay via Transistor (44).

Energized D.C. Lock-Out relay transfers two relay contacts. . . . One operates the Audio Control relay (45) which turns on the Wall Box speakers.

The second relay. contact in addition to removing the "hold" signal from the "Divide" Counter (8), connects a circuit to every Wall Box A.C. Lock-Out relay (46) in the system.

The Lock-Out relay contact (47) in each wall box provides a "hold" circuit for all wall box selections to the system except the one in operation. This prevents overlapping of selections from other wall boxes causing a wrong selection.




1 AMP
SLO-BLO
WHT
25V.A.C.
POWER SUPPLY
GRN-BLK
WHT-ORN
GRN-BLK
D1
D2
D3
D4
RED-YEL
TO REGULATOR
C5
.1
MFD
C1
1000
MFD
"CLOCK GENERATOR"
Q4
R16
22K
C8
.1
MFD
R17
470K
A10
C7
2200
PF
5V.D.C.
FROM REGULATOR
A9
CREDIT
SW. #2
CARRY-
OVER
SW.
D.C.
LOCK-
OUT
RE.
TO GROUND VIA
AUDIO CONTROL RE.
2ND
DIGIT
LITE
WHT-
BLK
47Ω
WHT-
GRN
Q6
"0"
R11
22K
R10
10K
5V.
TRANSISTOR
RECEIVER
RELAY TYPE
RECEIVER
R21
22K
50
Q10
D7
R19
2.2K
51
Q9
R20
68Ω
C12
.1
R22
2.2K
R29
22K
OZ1 IN4758
3-4-10-11
8
"HOLD" CIRCUIT REMOVED
(FROM D.C. LOCKOUT RELAY)
MC4023
A12
100
MS.
50
MS.
DIVIDE BY 10-50HZ
OR 12-60HZ
B19
"1"
"0"
55
B20
49
NOTE:
DURING TRANSMISSION INPUTS (A) AND (B)
REMAIN IN A "1" STATE.
48
B5
B12
B13
B18
B10
DIGIT STEP
COUNTER
1ST
PULSE
TRAIN
ENABLE
1ST
PULSE TRAIN
GENERATOR
16
5V.
B9
54
52
2ND PULSE TRAIN
ENABLE
B2
TO 2ND PULSE TRAIN GENERATOR
53

SEQUENCE No. 8
TRANSMISSION OF THE
1st PULSE TRAIN

The "hold" circuit now removed from the Divide Counter (8), starts to transmit the oscillations from the Clock Generator.

The signal oscillates at a rate of 120 cps. As the oscillations transmit thru the Divide Counter the gating is such that the pulse rate is reduced to 10 cps., (120 ÷ 12) which is the desirable pulsing rate to operate the Receiver.

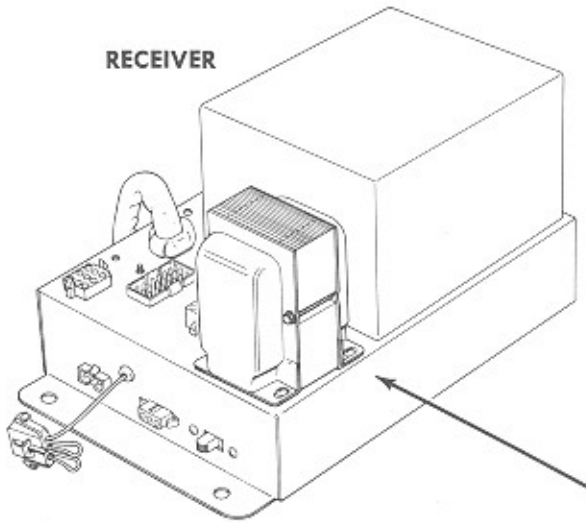
One input of the 1st Pulse Train NAND gate (48) is clamped to a "1" state provided by the output of NOR gate "S4". The 2nd input receives the "up-down" signal levels from the Divide Counter. The output of NAND gate (48) reproduces the pulsing transmission and triggers the 1st Pulse Train Generator into a switching sequence until the stored code of 1-0-0-0-1 is toggled to 0-0-0-0-0.

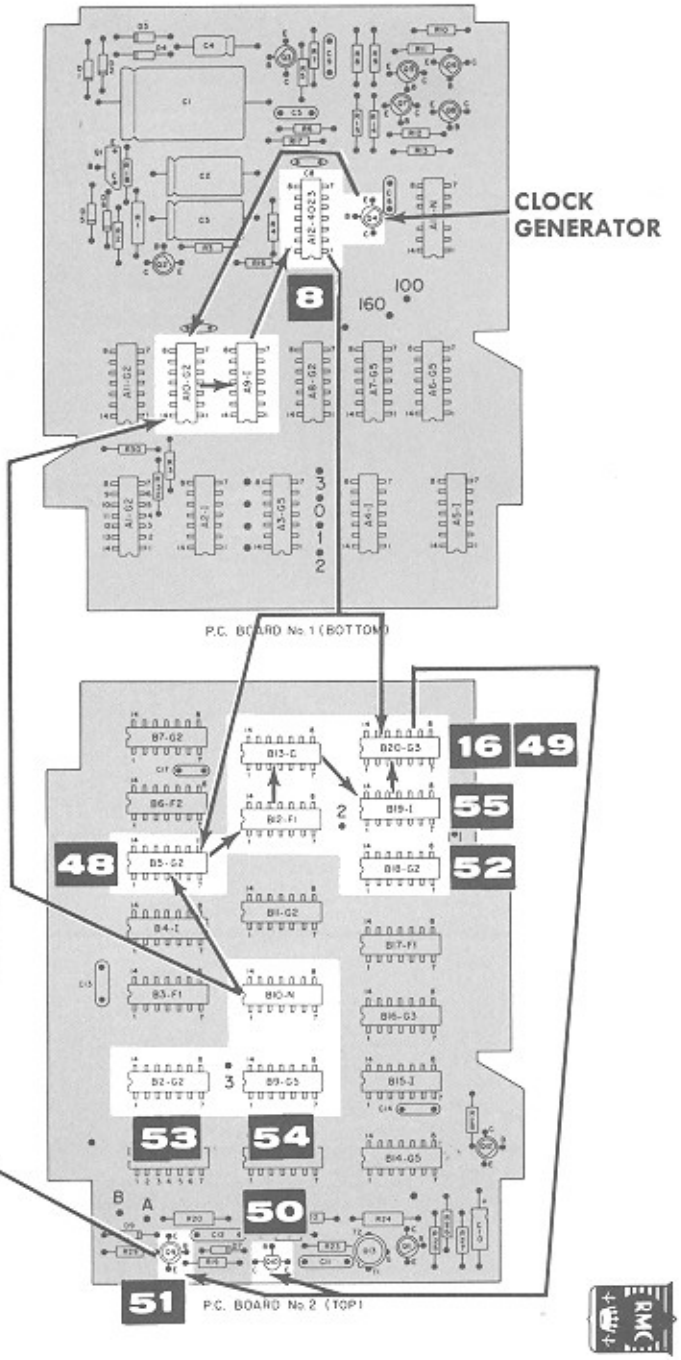
During this switching sequence, 10 pulses in the 1st Pulse Train are transmitted from the output of NAND gate (49) and applied to Transistors (50) & (51). Outputs of the Transistor circuits are designed to key either a transistorized or relay type Receiver. See Receiver Consideration on page 5.

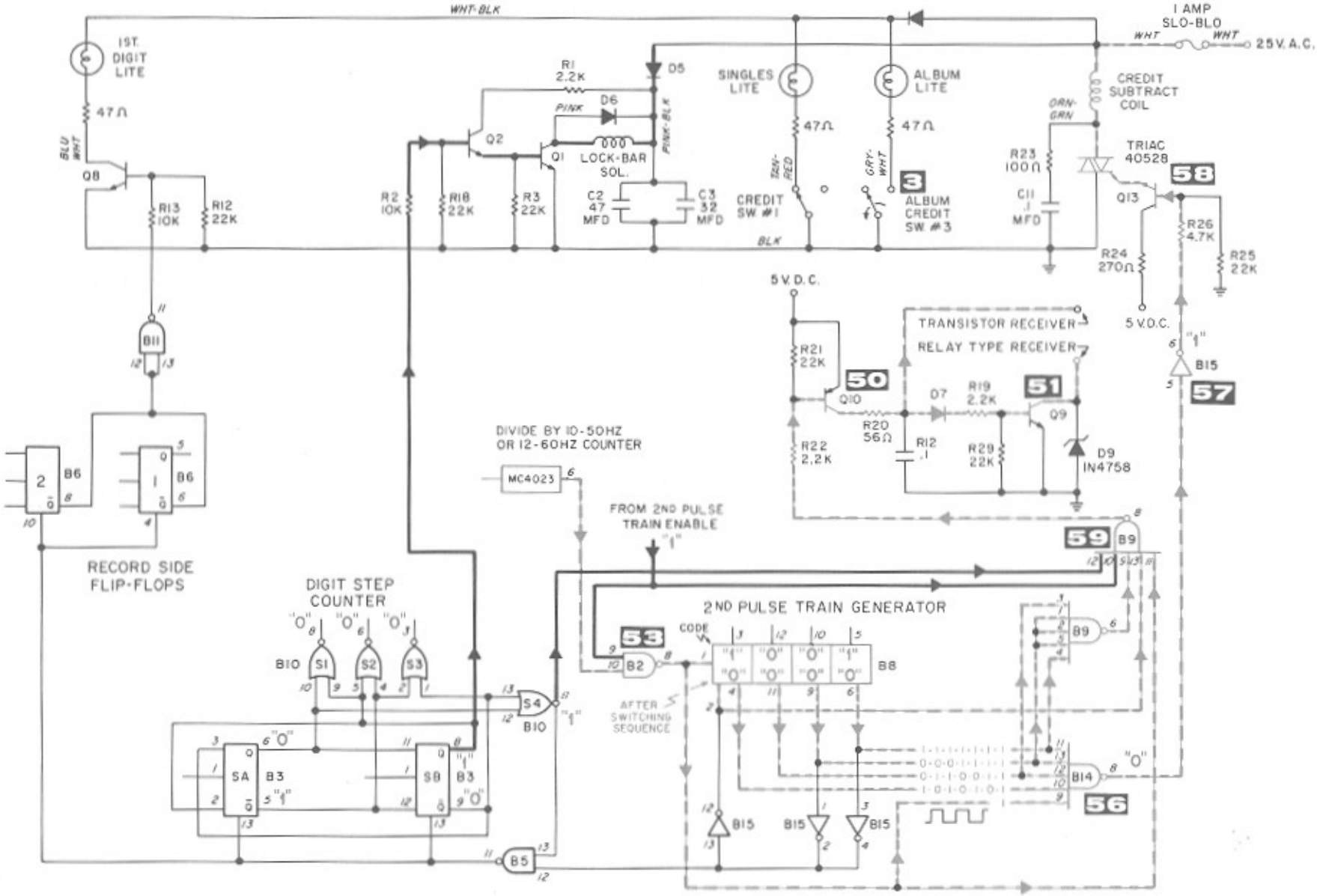
Since all FLIP-FLOPS in the 1st Pulse Train Generator returned to a "O" state, the outputs of the 5 INVERTERS in the network become "1" causing two actions to take place.

1. The output of gate (16) changes to "O" and clamps the Generator to its original standby condition.
2. The output of the 2nd Pulse Train NAND gate (52) changes to "1" via the network in the circuit setting up a logical "1" at one input of NAND gate (53) & (54). The 2nd Pulse Train Generator is ready to start transmission after a time delay of approximately 200 milliseconds.

The "O" output of INVERTER (55) shuts off the Transistor in the circuit . . . 2nd Digit lite turns off.






WHT-BLK
1 AMP SLO-BLO
WHT
WHT
25 V. A.C.
1ST. DIGIT LITE
47Ω
BLU WHT
Q8
R13 10K
R12 22K
R1 2.2K
D5
D6
PINK
PINK-BLK
Q2
Q1
LOCK-BAR SOL.
R2 10K
R18 22K
R3 22K
C2 47 MFD
C3 32 MFD
SINGLES LITE
ALBUM LITE
47Ω
47Ω
TAN-RED
GRY-WHT
CREDIT SW #1
3
ALBUM CREDIT SW #3
BLK
CREDIT SUBTRACT COIL
ORN-GRN
R23 100Ω
C11 .1 MFD
TRIAC 40528
58
Q13
R26 4.7K
R25 22K
R24 270Ω
5 V.D.C.
5 V.D.C.
R21 22K
50
Q10
R20 56Ω
R22 2.2K
R12 .1
TRANSISTOR RECEIVER
RELAY TYPE RECEIVER
D7
R19 2.2K
51
Q9
R29 22K
D9 IN4758
"1"
B15
57
B11
DIVIDE BY 10-50HZ OR 12-60HZ COUNTER
MC4023
FROM 2ND PULSE TRAIN ENABLE
"1"
59
B9
RECORD SIDE FLIP-FLOPS
2
B6
1
B6
DIGIT STEP COUNTER
"0"
"0"
"0"
B10
S1
S2
S3
S4
B10
"1"
SA
B3
"0"
"1"
SB
B3
"1"
"0"
B5
2ND PULSE TRAIN GENERATOR
53
CODE
B2
B8
AFTER 5 SWITCHING SEQUENCE
B9
B14
"0"
56
B15
B15
B15

SEQUENCE No. 9
TRANSMISSION OF THE 2nd TRAIN—1 CREDIT REMOVED

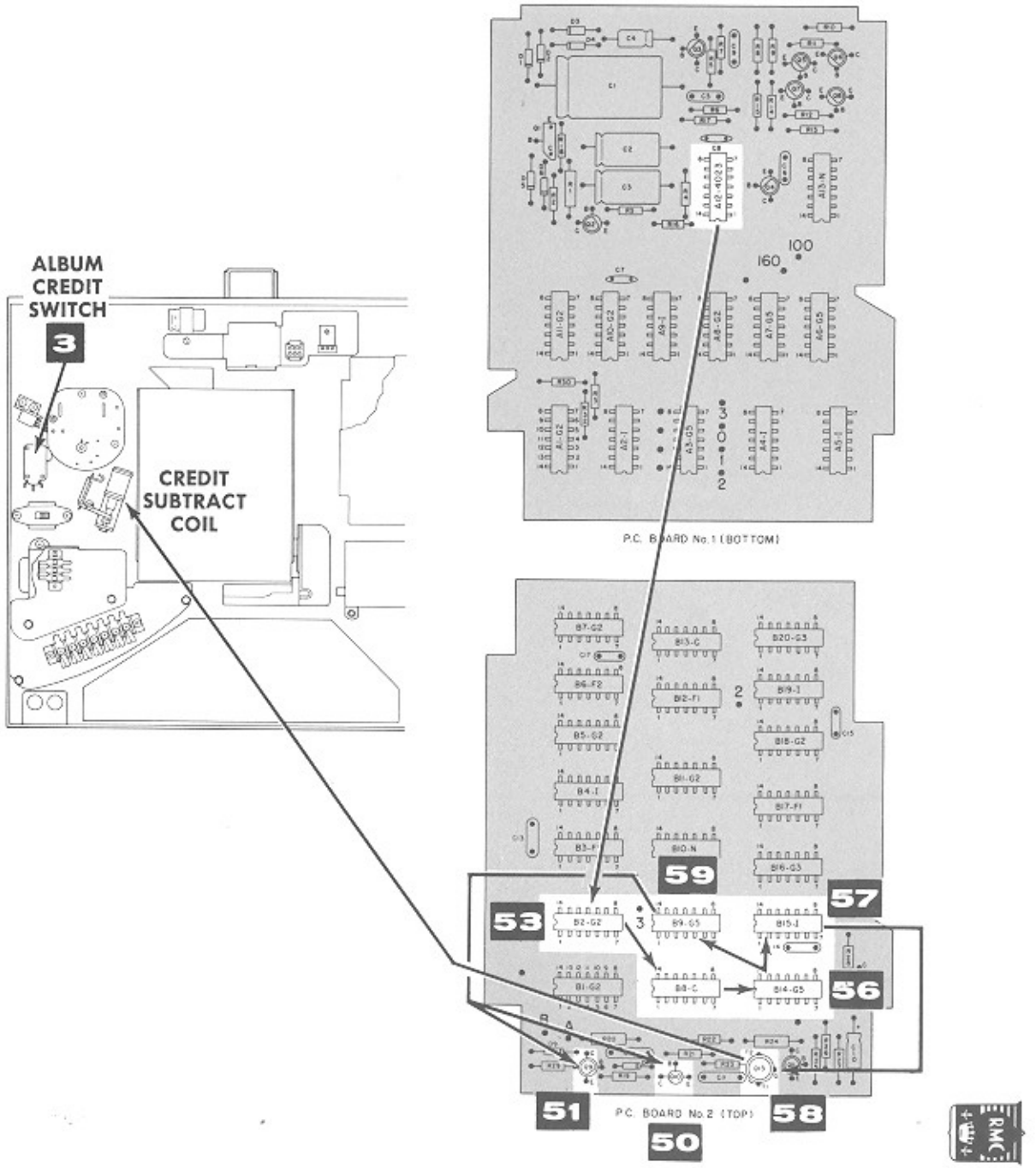
After the 200 millisecond delay interval between the 1st and 2nd pulse train the 2nd Pulse Train Generator is activated.

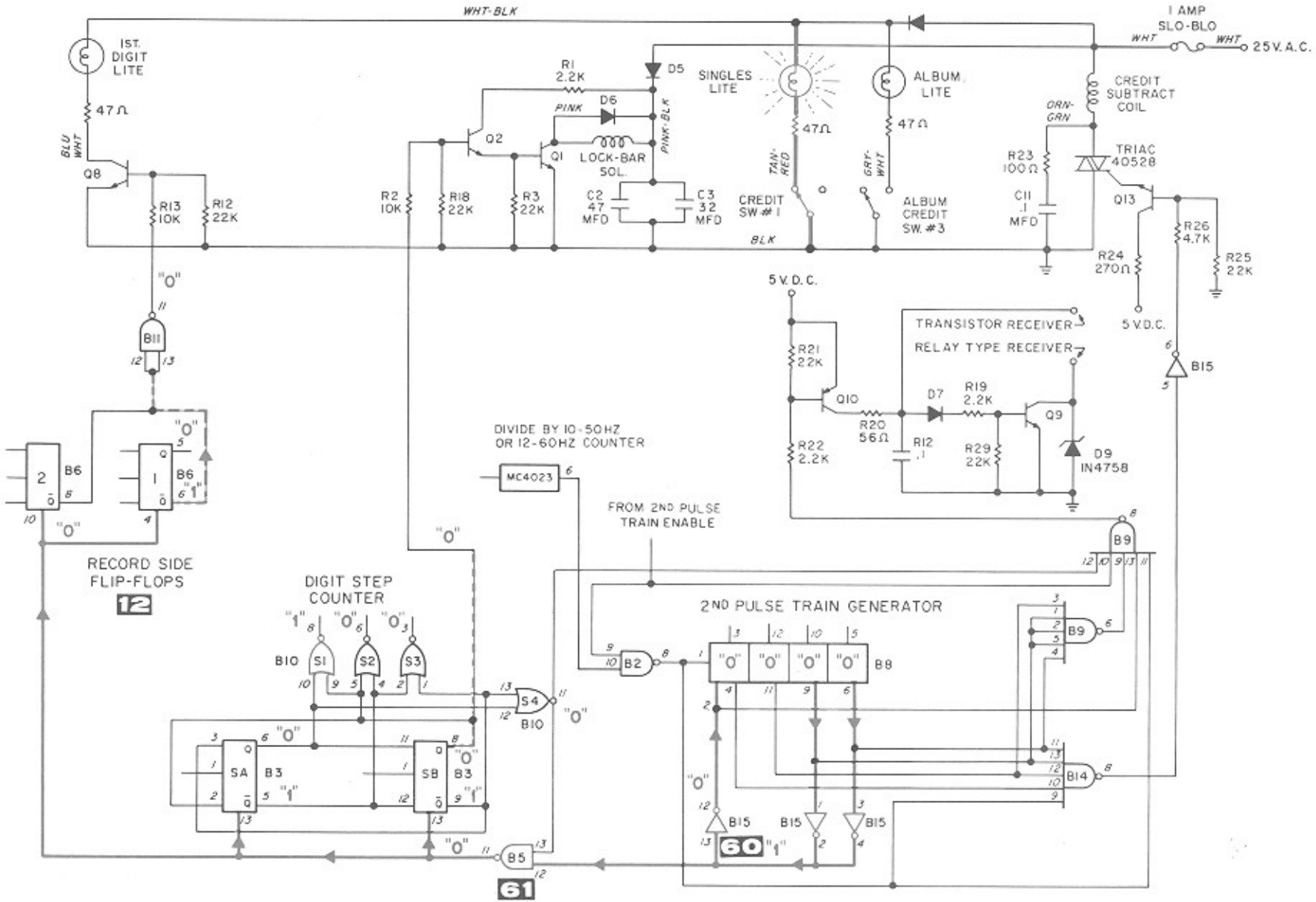
The second input of NAND gate (53) receives the "up-down" transmission from the "Divide by 10 or 12" Counter. Output of NAND gate (53) reproduces the rise and fall of the clock pulse and triggers the 2nd Pulse Train Generator into a switching sequence until the stored code of 1-0-0-1 is toggled to 0-0-0-0.

During the switching sequence, two actions take place.

1. The 5 inputs of NAND gate (56) change in sync with the shifting of "O" and "1" logic of each FLIP-FLOP in the 2nd Pulse Train Generator.
   At the end of the 2nd pulse train the 5 inputs of NAND gate (56) are shifted to a "1" state for a one pulse interval.
   The "O" output pulse, after passing thru INVERTER (57), changes to "1" and triggers the Transistor–Triac network (58). Credit Subtract Coil energizes removing one credit from the Master Ratchet. . . . Album Credit Switch (3) returns to a "less than two credits" position. Album Select lite goes out.

2. During the above action four pulses in the 2nd Pulse Train are transmitted from the output of NAND gate (59) and applied to Transistors (50) and (51).
   Outputs of the Transistors key the Receiver as explained in the previous Sequence.




WHT-BLK
1 AMP SLO-BLO
WHT
WHT
25 V. A. C.
1ST. DIGIT LITE
47Ω
BLU WHT
Q8
R13 10K
R12 22K
R1 2.2K
D5
D6
PINK
PINK-BLK
Q2
Q1
LOCK-BAR SOL.
C2 47 MFD
C3 32 MFD
R2 10K
R18 22K
R3 22K
SINGLES LITE
ALBUM LITE
47Ω
47Ω
TAN-RED
GRY-WHT
CREDIT SW. #1
ALBUM CREDIT SW. #3
BLK
CREDIT SUBTRACT COIL
ORN-GRN
R23 100Ω
C11 .1 MFD
TRIAC 40528
Q13
R24 270Ω
R26 4.7K
R25 22K
5 V.D.C.
5 V.D.C.
TRANSISTOR RECEIVER
RELAY TYPE RECEIVER
R21 22K
Q10
R20 56Ω
R12 .1
D7
R19 2.2K
Q9
R29 22K
D9 IN4758
R22 2.2K
B15
"0"
B11
DIVIDE BY 10-50HZ OR 12-60HZ COUNTER
MC4023
FROM 2ND PULSE TRAIN ENABLE
B9
RECORD SIDE FLIP-FLOPS
12
DIGIT STEP COUNTER
"1"
"0"
"0"
B10
S1
S2
S3
S4
SA
SB
B3
B3
2ND PULSE TRAIN GENERATOR
B2
B8
B9
B14
B15
B15
B15
60
"1"
B5
61

SEQUENCE No. 10
SYSTEM RESETS

When the 2nd Pulse Train Generator is returned to a "O" state, INVERTER (60) output is driven "O" via the two paralleled INVERTERS in the circuit and clamps the 2nd Pulse Train Generator to its original standby or "O" state.

At the same time, NAND gate (61) output is driven "O" and resets the Q outputs of "Record Side" FLIP-FLOPS (12), and Digit Step Counter FLIP-FLOP "SB" to standby or "O".

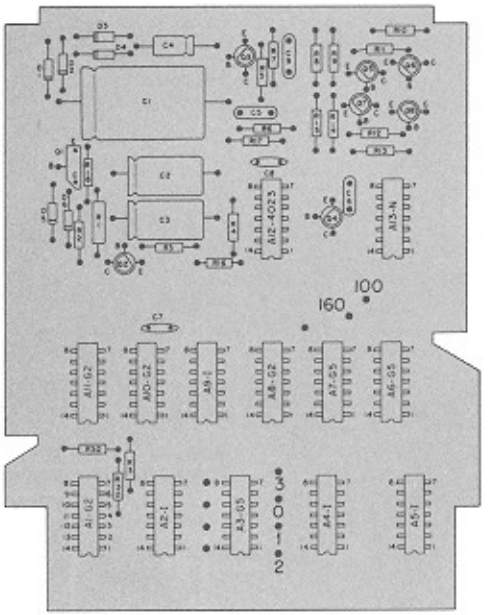
The "1" state $\overline{Q}$ output of "Record Side" FLIP-FLOPS (12) shut-off the Transistor in the circuit, . . . 1st Digit lite goes out.

The "O" output of "SB" disconnects power to the Lock Bar Solenoid releasing the "held" P.B. switch.

Since one credit is still stored in the accumulator, "Singles" lamp remains lit and the "1" output state of NOR gate "S4" is advanced to NOR-gate "S1". The system is now ready to accept the next "Single" record selection.

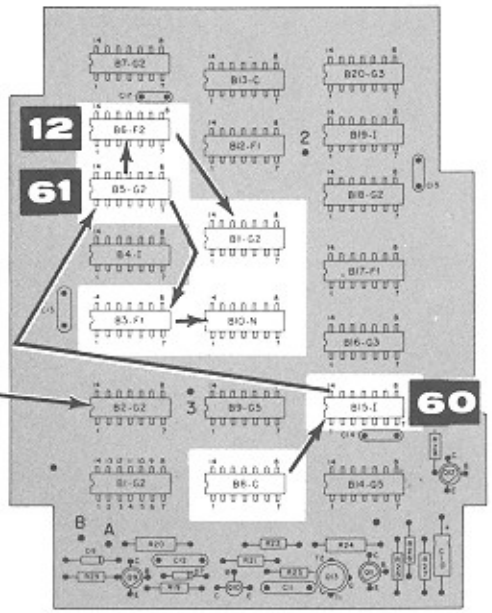
If no credits are registered in the accumulator, all credit switches transfer to a open position removing power from the selection system.

Wall Box now at standby and ready to receive coins.

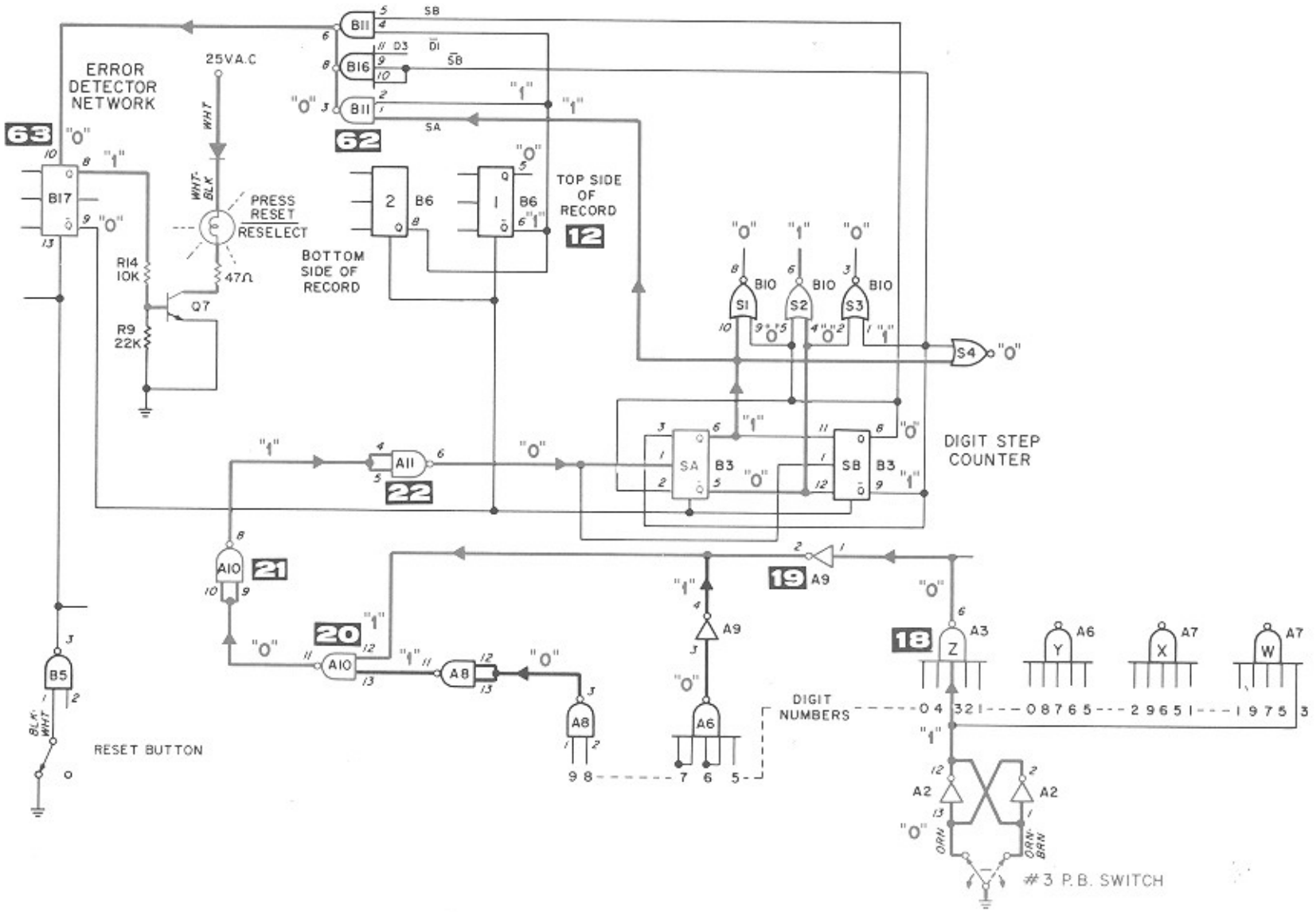


P.C. BOARD No. 1 (BOTTOM)

CAUTION: When replacing I.C.'s, the reference mark (notch) must point in the same direction as indicated by the associated I.C. packages on the P.C. board. Failure to do so will destroy the I.C.



P.C. BOARD No. 2 (TOP)


ERROR DETECTOR NETWORK
25VA.C
WHT
WHT-BLK
PRESS RESET RESELECT
R14 10K
47Ω
Q7
R9 22K
63
62
12
TOP SIDE OF RECORD
BOTTOM SIDE OF RECORD
DIGIT STEP COUNTER
22
21
20
19
18
DIGIT NUMBERS
04321---08765---29651---1975 3
RESET BUTTON
#3 P.B. SWITCH

SEQUENCE No. 11
ERROR NUMBER SELECTED FOR 1st DIGIT

When a wrong 1st Digit number is pressed, as P.B. #3, record side FLIP-FLOPS (12) are not activated and the state of Q output remains "1".

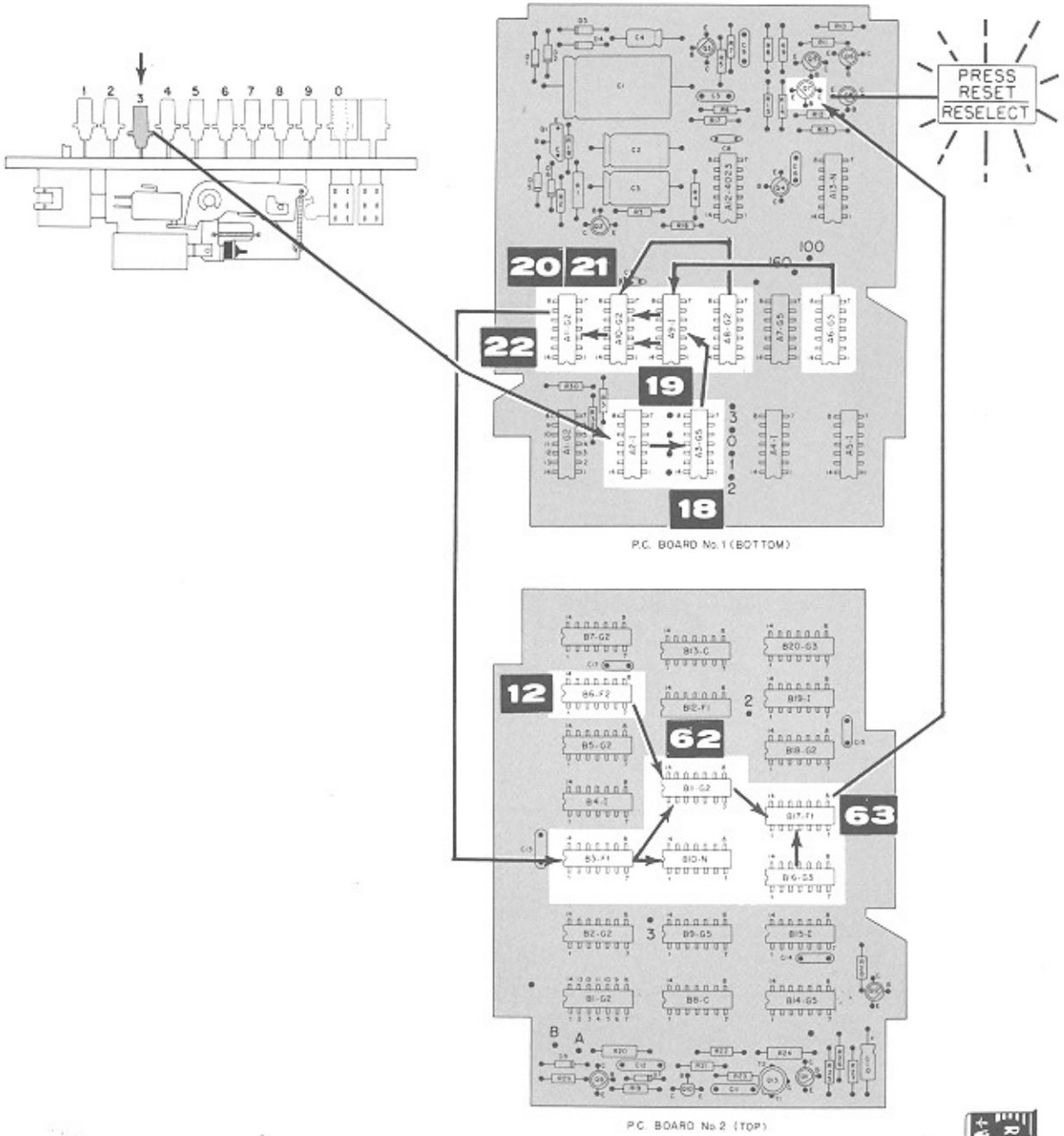
The $\bar{Q}$ is connected to one input of NAND gate (62) in the Error Detector Network and will effect a "no go" condition when the P.B. switch returns.

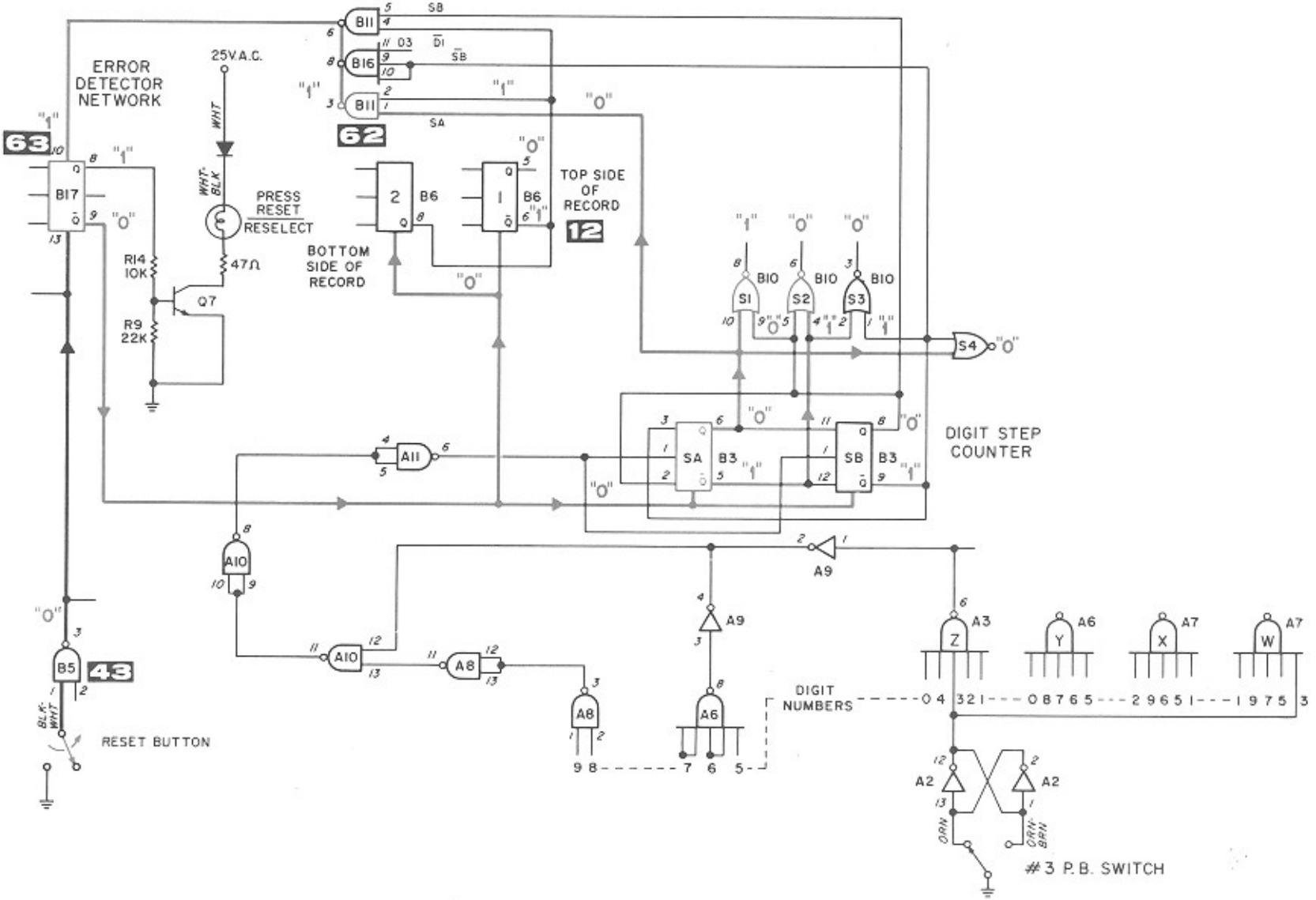
The error is detected in the following manner:

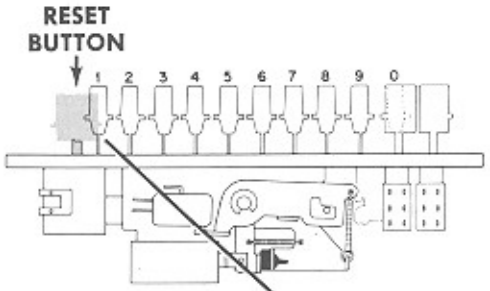
The "up" stroke of the P.B. switch activates the Digit Step Counter line of a INVERTER and NAND gates (18 thru 22), tripping the "SA" Q output to "1" and $\bar{Q}$ to "O". This causes the "1" output state of NOR gate "S1" to transfer to NOR gate "S2". At the same time the "1" state output of "SA" is applied to the second input of NAND gate (62) causing the "O" output to trigger FLIP-FLOP (63).

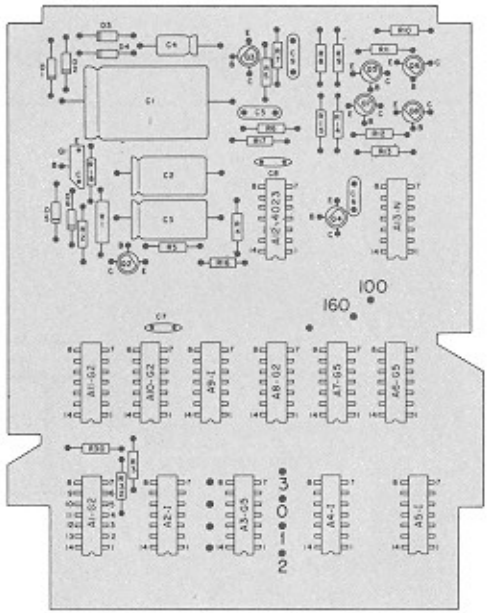
The "Q" output of FLIP-FLOP (63) changes to "1" which turns on the Transistor in the circuit, . . . " Reset and Reselect" lamp lites.

The "$\bar{Q}$" output of FLIP-FLOP (63) changes to "O" and its function is explained in the next sequence.

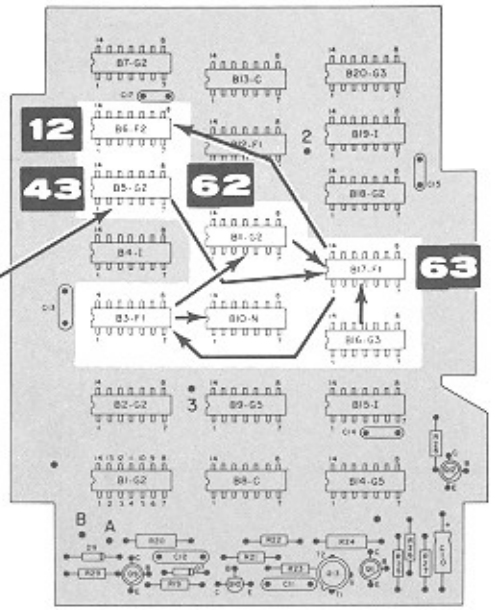



ERROR DETECTOR NETWORK
25V.A.C.
WHT
WHT-BLK
PRESS RESET
RESELECT
47Ω
R14 10K
R9 22K
Q7
63
B17
62
B11
B16
B11
SB
SA
DI
03
TOP SIDE OF RECORD
BOTTOM SIDE OF RECORD
12
B6
B6
S1
S2
S3
S4
BIO
DIGIT STEP COUNTER
SA
SB
B3
A11
A10
A8
A9
A6
A3
A7
Z
Y
X
W
DIGIT NUMBERS
04321---08765---29651---1975 3
98-------765
B5
43
BLK-WHT
RESET BUTTON
A2
ORN
ORN-BRN
#3 P.B. SWITCH





P.C. BOARD No 1 (BOTTOM)



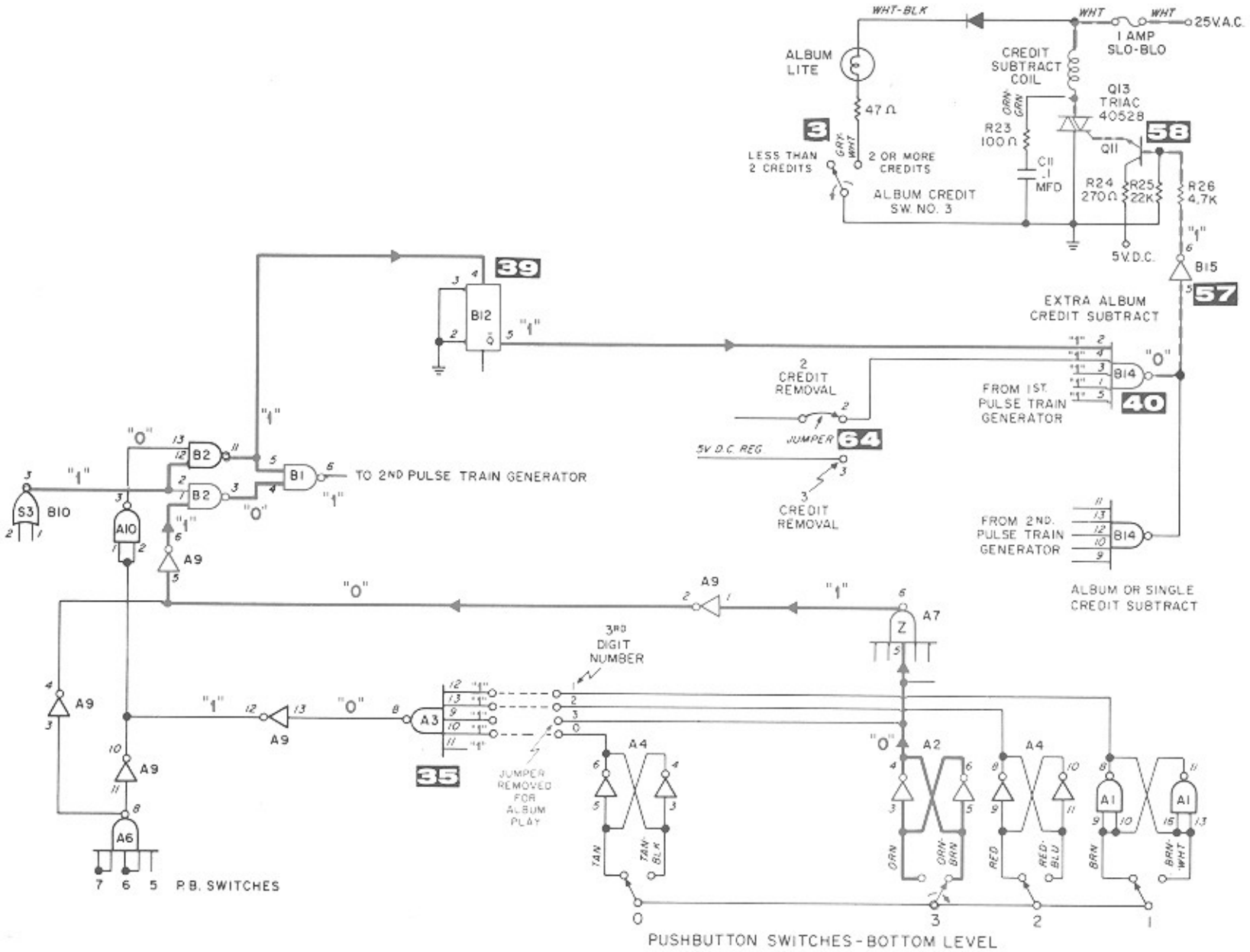
P.C. BOARD No 2 (TOP)

SEQUENCE No. 12
SYSTEM CLAMPED IN ERROR STATE— RESET BUTTON PRESSED

The Reset Line from $\overline{Q}$ of FLIP-FLOP (63) now changed to "O" resets the Digit Step Counter to its original standby state. The Q output of "SA" now "O" causes the output NAND gate (62) in the Error Detector Network to change to "1" which locks-up FLIP-FLOP (63) and Record Side FLIP-FLOPS (12) in an error condition. No selections will now be accepted until the error condition is cleared.

Pressing the Reset Button changes the output of NAND gate (43) to "O" which is the trigger to reset the entire selection system to standby.

Reset lite goes out and the system is now ready to accept the correct 1st Digit number.


WHT-BLK
WHT
WHT
25V.A.C.
1 AMP SLO-BLO
ALBUM LITE
47 Ω
CREDIT SUBTRACT COIL
Q13 TRIAC 40528
ORN GRN
R23 100Ω
C11 .1 MFD
Q11
58
3
GRY WHT
LESS THAN 2 CREDITS
2 OR MORE CREDITS
ALBUM CREDIT SW. NO. 3
R24 270Ω
R25 22K
R26 4.7K
5V.D.C.
B15
57
EXTRA ALBUM CREDIT SUBTRACT
39
B12
"1"
"0"
B14
40
2 CREDIT REMOVAL
JUMPER 64
5V D.C. REG
3 CREDIT REMOVAL
FROM 1ST. PULSE TRAIN GENERATOR
FROM 2ND. PULSE TRAIN GENERATOR
ALBUM OR SINGLE CREDIT SUBTRACT
B1
B2
TO 2ND PULSE TRAIN GENERATOR
S3 B10
A10
A9
A7
Z
3RD DIGIT NUMBER
A3
35
JUMPER REMOVED FOR ALBUM PLAY
A4
A2
A1
A6
7 6 5 P.B. SWITCHES
TAN
TAN BLK
ORN
ORN BRN
RED
RED BLU
BRN
BRN WHT
0 3 2 1
PUSHBUTTON SWITCHES - BOTTOM LEVEL

SEQUENCE No. 13
ALBUM/SINGLES PROGRAMMING AND CREDIT REMOVAL

Album/Singles NAND gate (35) provides for programming "Album" and "Single" records to two different rates of credit removal.

Four of the NAND gate inputs have a jumper arrangement, each representing an Album program group of 20 selections that end with the 3rd Digit "O"–"1"–"2" or "3".

When the four jumpers are connected, the selection system is set up for "Singles" play only and subtraction of 1 credit.

The four inputs may be disconnected in any sequence of 20 selections for Album play which also sets the credit system to a 2 credit subtraction. For a 3 credit subtraction, (after presetting the 25¢ ratchet in the accumulator, remove the jumper (64) from the 2 credit pin and move it to the 3 credit pin.

REFERENCE TABLE

NAND GATE (35) Input	Program Group Ending with 3rd Digit Number
0	0–1st Program Group
1	1–2nd Program Group
2	2–3rd Program Group
*3	3–4th Program Group

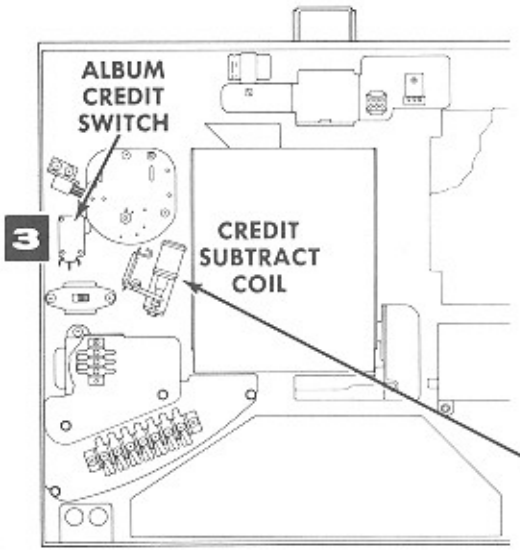
* Example: Jumper removed from input 3 . . . 4th Program Group of 20 selections ending with Digit number "3" set to play Album records to a 25¢ base and subtraction of 2 credits.

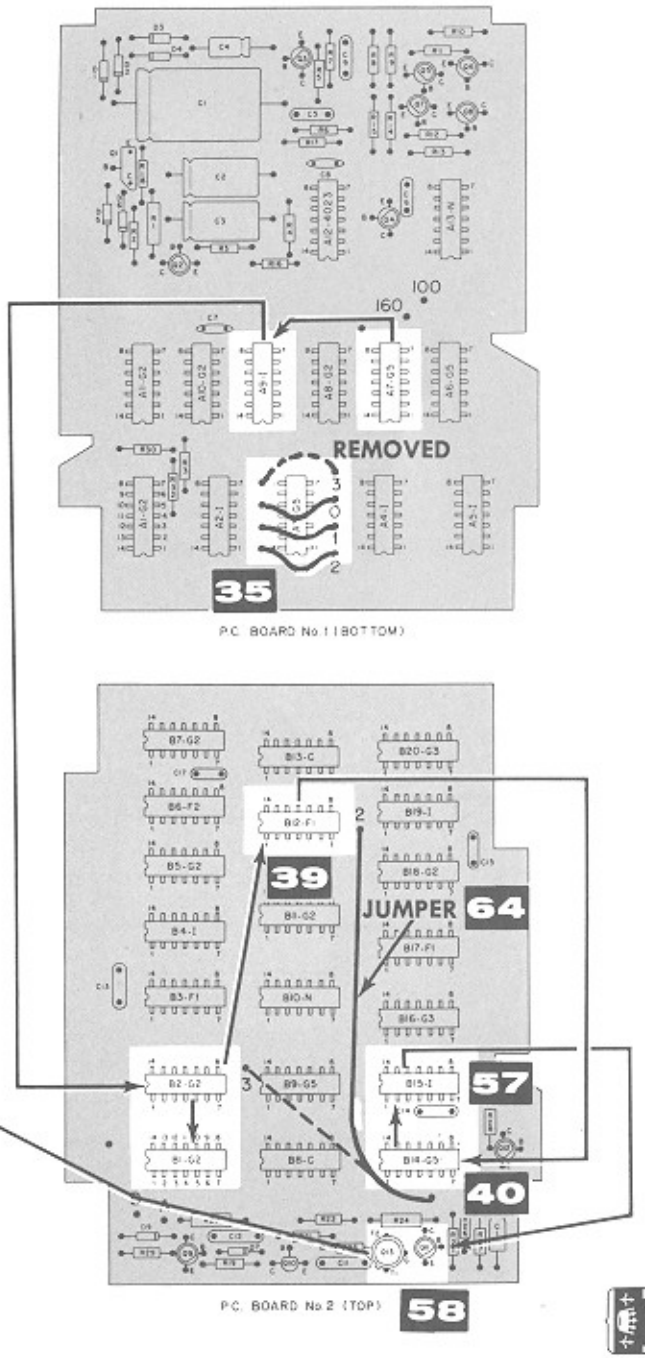
Upon pressing P.B. switch #3, the output of NAND gate (35) remains "O" which results in the Q and $\overline{Q}$ of FLIP-FLOP (39) to remain unchanged.

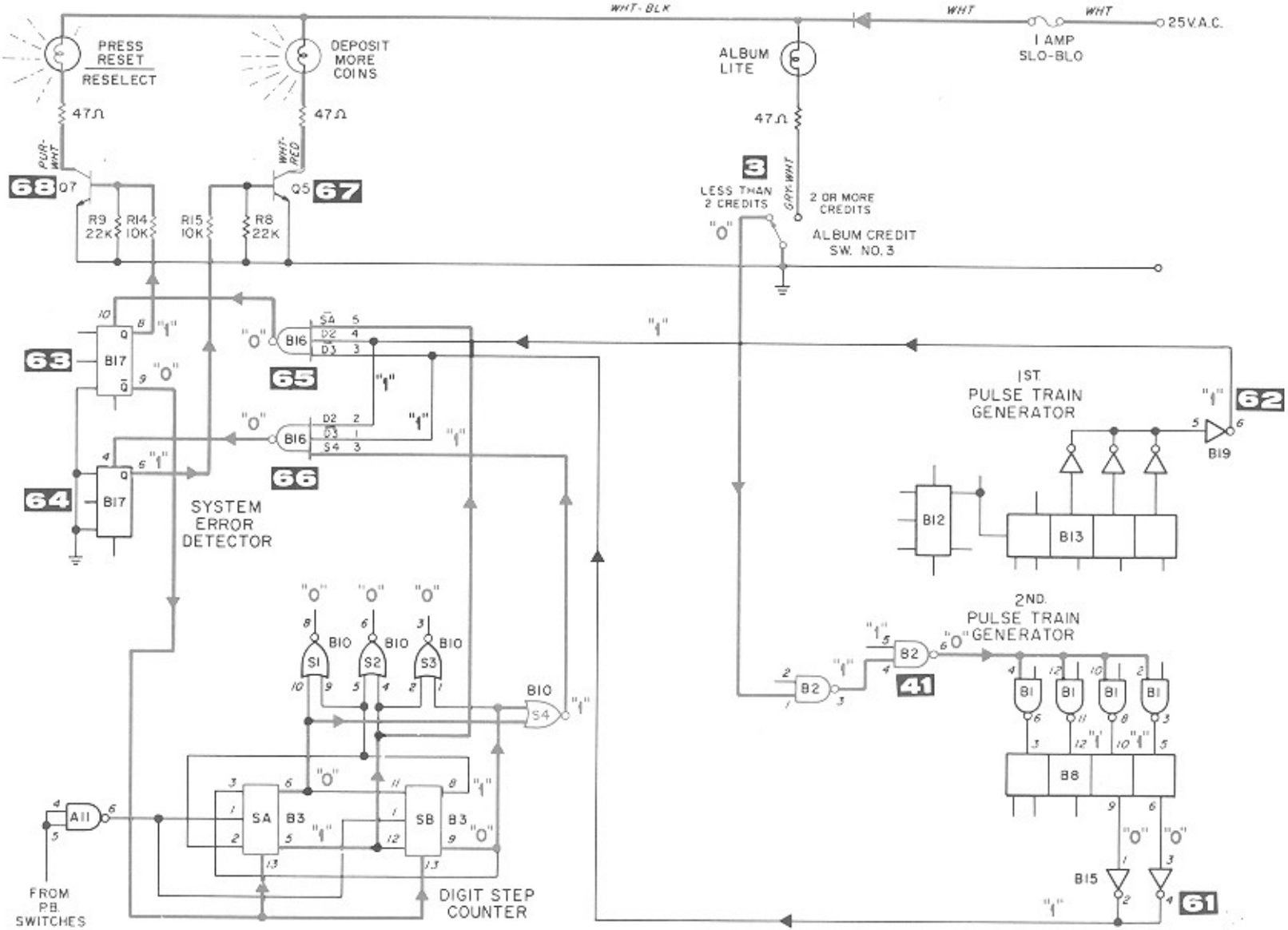
The "1" of $\overline{Q}$ is clamped to one input of NAND gate (40). At the end of the 1st Pulse Train Transmission to the Receiver, the four remaining NAND gate inputs are toggled to a "1" state for a one pulse interval.

The one pulse "O" output, after passing thru INVERTER (57), changes to "1" which triggers Transistor-Triac network (58) to remove the 1st credit from the accumulator. . . . Album Credit Switch (3) returns to a "less than 2 credits" position, . . . Album select lite turns off.

The 2nd Credit subtraction takes place at the end of the 2nd Pulse Train as explained in Sequence No. 9.






WHT-BLK
WHT
WHT
25V.A.C.
1 AMP SLO-BLO
PRESS RESET RESELECT
DEPOSIT MORE COINS
ALBUM LITE
47Ω
47Ω
47Ω
PUR-WHT
WHT-RED
GRY-WHT
68
Q7
Q5
67
R9 22K
R14 10K
R15 10K
R8 22K
3
LESS THAN 2 CREDITS
2 OR MORE CREDITS
ALBUM CREDIT SW. NO. 3
63
B17
64
B17
65
B16
66
B16
SYSTEM ERROR DETECTOR
1ST PULSE TRAIN GENERATOR
62
B19
B12
B13
2ND. PULSE TRAIN GENERATOR
41
B2
B2
B1
B8
B15
61
S1
S2
S3
S4
B10
SA
SB
B3
A11
FROM P.B. SWITCHES
DIGIT STEP COUNTER

SEQUENCE No. 14
INSUFFICIENT CREDITS—
ALBUM SELECTION MADE

Should the 3rd Digit number be pressed to play an "Album" tune and the Album Credit Switch (3) is in a "less than 2 credits" position, the "O" output of NAND gate (41) clamps the 2nd Pulse Train Generator into a "no go" condition. The "1" state output of "S3" in the Digit Step Counter however transfers to "S4".

The "1" state outputs of NOR gate "S4" and INVERTERS (61) and (62) are applied to the input of NAND gates (65) and (66) in the Error Detector Network.

Since all NAND gate inputs now are in a "1" state, the outputs change to "O" and set the Q outputs of FLIP-FLOP (63) and (64) to "1" and $\overline{Q}$ to "O".

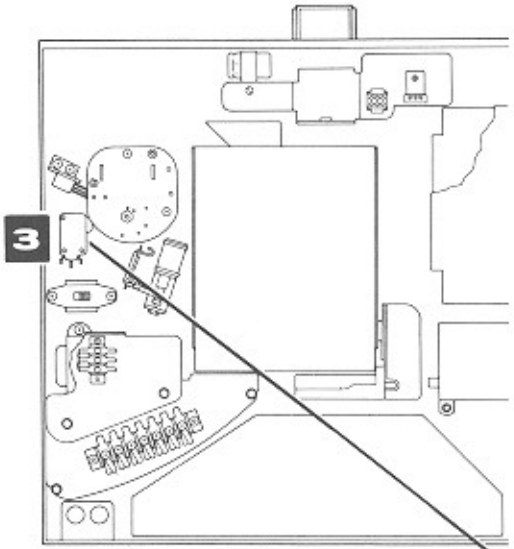
Q "1" of FLIP-FLOP (64) drives Transistor (67) which turns on "Deposit More Coins" lite.

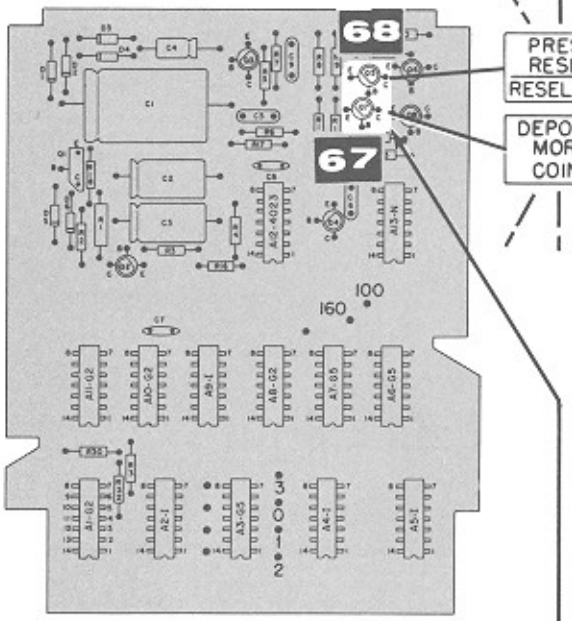
Q "1" of FLIP-FLOP (63) drives Transistor (68) which turns on "Reset and Reselect" lite.

$\overline{Q}$ "O" of FLIP-FLOP (63) locks-up the Step Counter disabling the selection system.

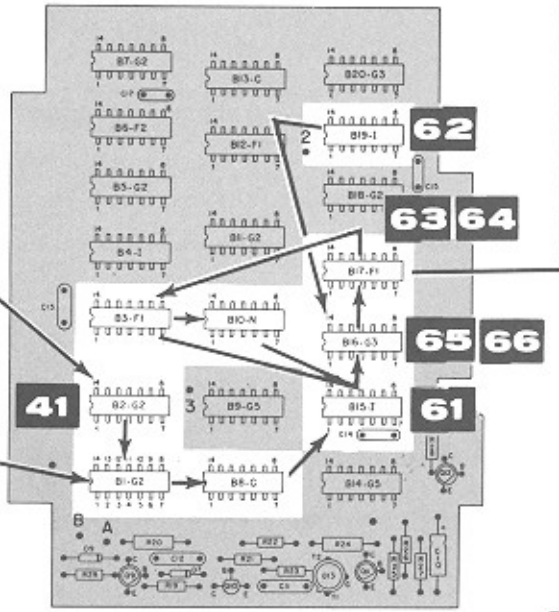
Adding more coins for an "Album" selection will not reset the system until the Reset Button is pressed to clear the "no go" condition.

The Album Tune can now be re-selected.



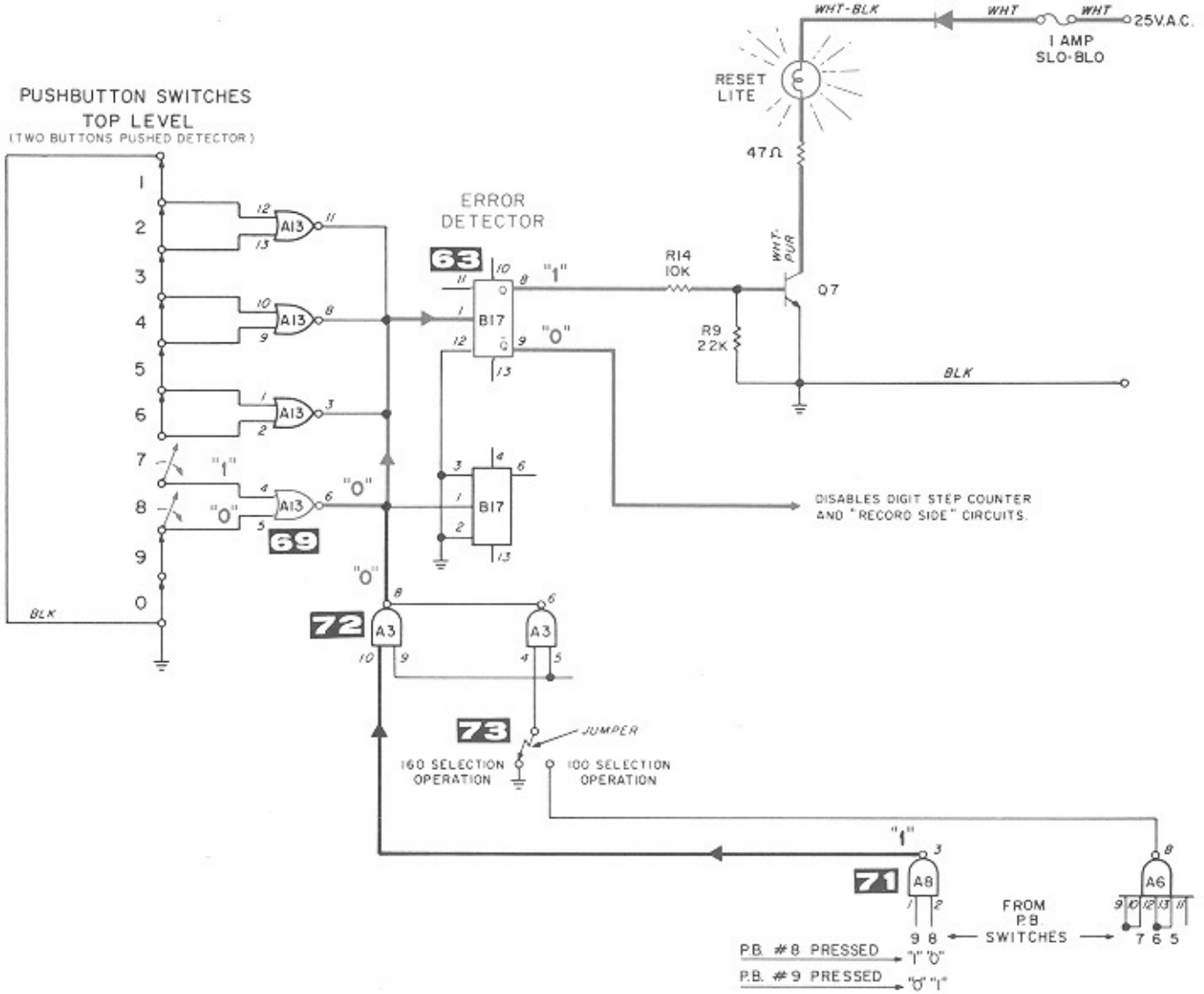


P.C. BOARD No 1 (BOTTOM)



P.C. BOARD No 2 (TOP)

CAUTION: When replacing I.C.'s, the reference mark (notch) must point in the same direction as indicated by the associated I.C. packages on the P.C. board. Failure to do so will destroy the I.C.


PUSHBUTTON SWITCHES
TOP LEVEL
(TWO BUTTONS PUSHED DETECTOR)
1
2
3
4
5
6
7
8
9
0
BLK
A13
A13
A13
A13
"1"
"0"
69
"0"
72
A3
A3
ERROR
DETECTOR
63
B17
B17
"1"
"0"
R14
10K
R9
22K
Q7
WHT-BLK
WHT
WHT
25V.A.C.
1 AMP
SLO-BLO
RESET
LITE
47Ω
WHT.
PUR
BLK
DISABLES DIGIT STEP COUNTER
AND "RECORD SIDE" CIRCUITS.
73
JUMPER
160 SELECTION
OPERATION
100 SELECTION
OPERATION
"1"
71
A8
A6
FROM
P.B.
SWITCHES
9 8
7 6 5
P.B. #8 PRESSED
"1" "0"
P.B. #9 PRESSED
"0" "1"

SEQUENCE No. 15

1. TWO OR MORE PUSHBUTTONS PRESSED OR

2. INCORRECT 3rd DIGIT NUMBER SELECTED

1. Pressing more than one digit number will cause the "Reset & Reselect" lamp to lite. The top level of P.B. switches are used for this purpose.

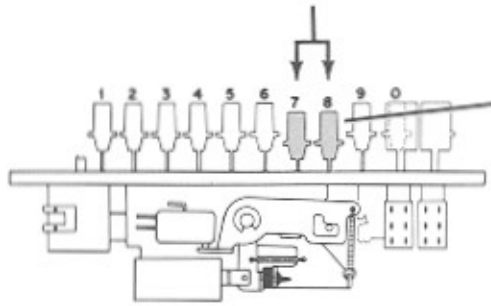
   P.B. switches #7 and #8 are shown depressed. P.B. switch #7 disconnects the ground circuit ("O" signal) from one input of NOR gate (69) causing it to become "1". The second input remains in a "O" state via the ground connection supplied by P.B. #9. The change in the input state of NOR gate (69) drives the output to "O" which is the trigger to activate the Error Detector FLIP-FLOP (63).

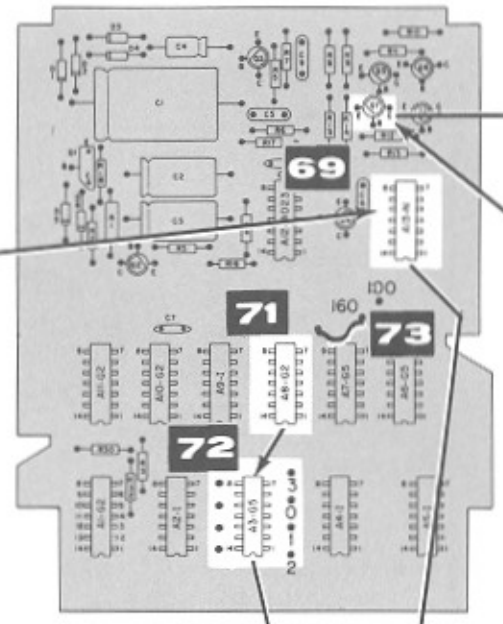
   The Q output of FLIP-FLOP (63) changes to "1" and turns on the Transistor in the circuit causing the Reset lamp to lite.

   The $\overline{Q}$ output changes to "O" and disables the selection system until cleared by pressing the Reset Button.

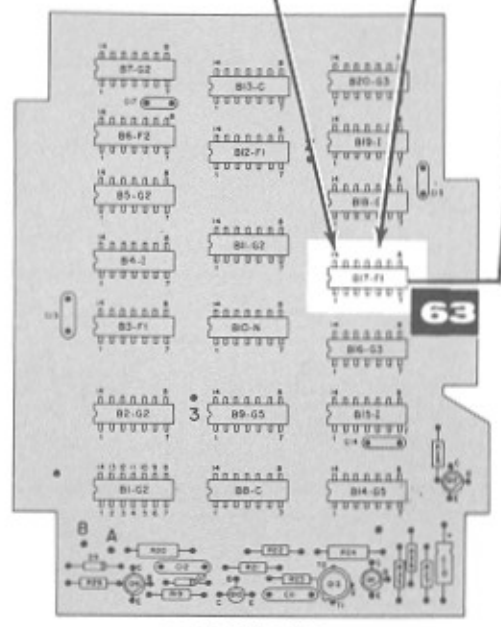
2. For 160 selection Wall Box operation the 3rd Digit numbers #8 and #9 are not valid. If pressed the output of NAND gate (71) in the P.B. switch circuit is driven to a "1" state and becomes "O" at the output of NAND gate (72). The "O" signal activates the Error Detector FLIP-FLOP (63) and disables the selection system as explained in the 1st example above.

   Note: For 100 selection operation the 3rd Digit numbers #5, #6, #7, #8 and #9 are not valid and disables the selection system via the "100 Selection Operation" jumper (73).

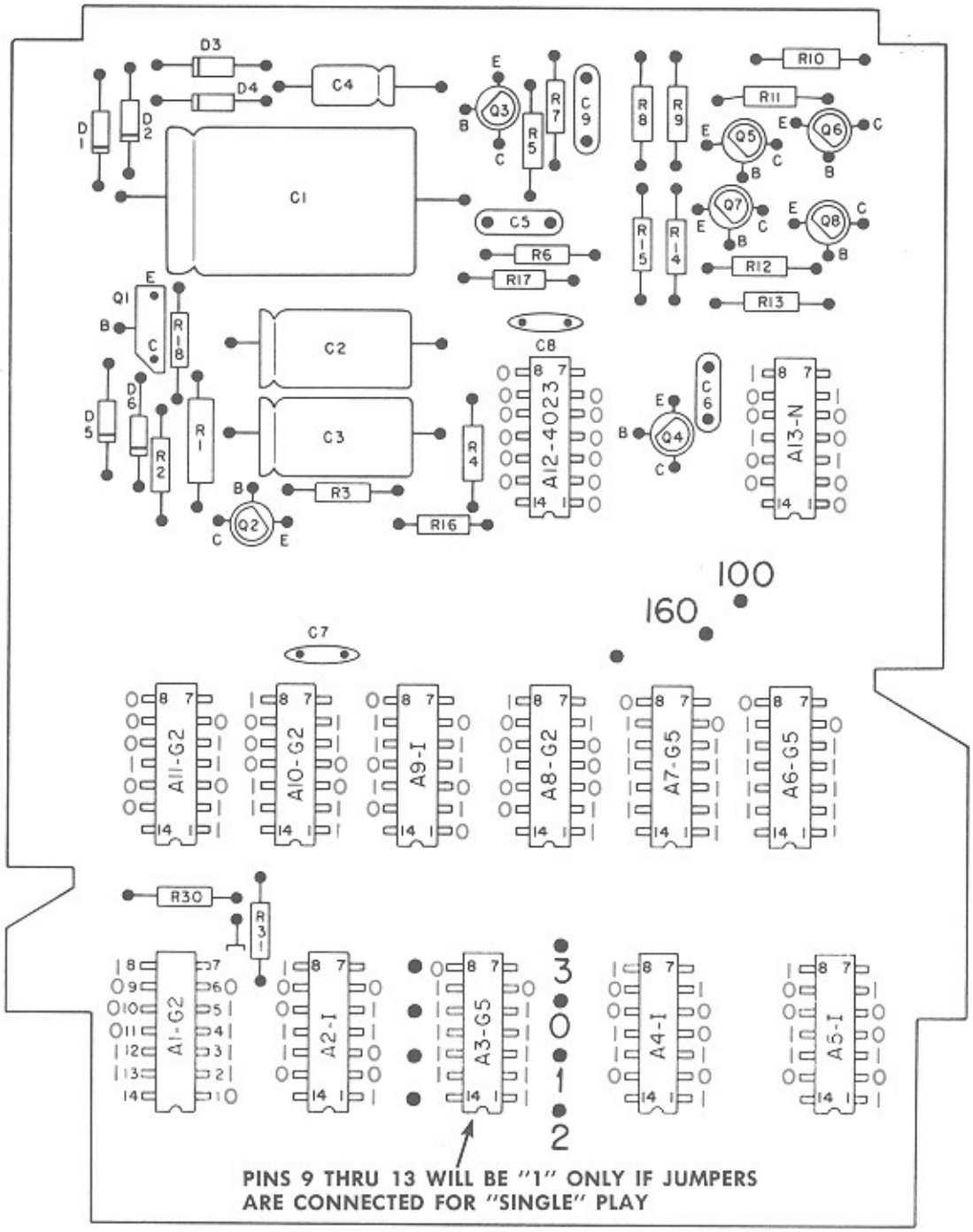




P.C. BOARD No. 1 (BOTTOM)



P.C. BOARD No. 2 (TOP)



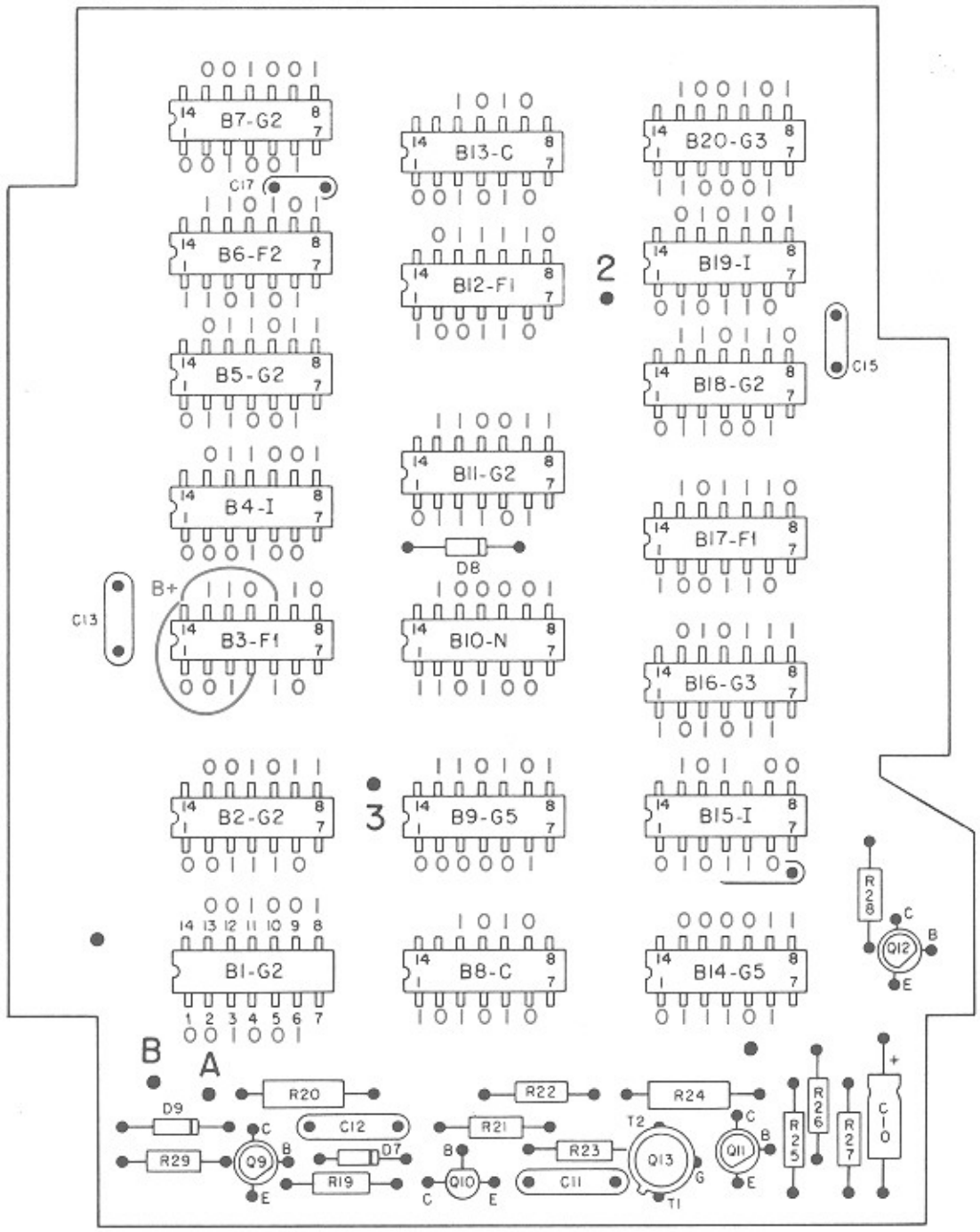
P.C. BOARD No. 1 (BOTTOM)

No. 47660-A

TROUBLE SHOOTING

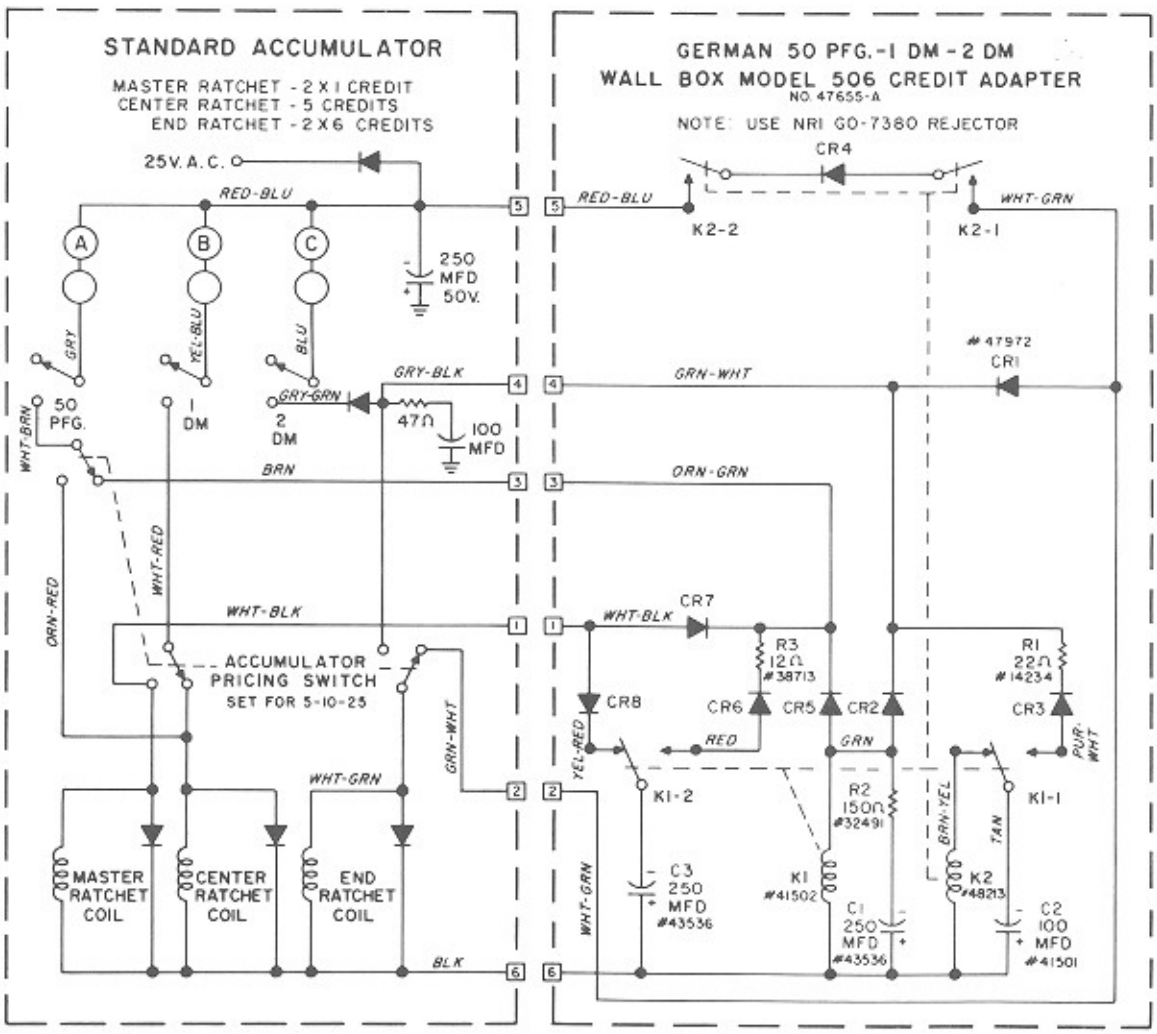
After a credit has been established the input and output state of each I.C. element sets to the signal level indicated at each pin.

The "O" signal level should be less than .5V.D.C. The "1" signal level should be between 3.6 to 5 V.D.C.



P.C. BOARD No. 2 (TOP)

No. 47665-A



GERMAN 50 PFG — 1 DM — 2 DM ADAPTER

The adapter is activated upon insertion of a 50 Pfg or 2 Dm which allows additional credits to be stored on the Master Ratchet. Use NRI Rejector GO – 7380

CYCLE OF OPERATION — 2 DM

1. Down stroke of the 2 Dm coin switch allows the end ratchet to register 6 credits via CR1. Relay K1 energizes and C1 charges thru R2 and CR2.

2. Relay contact K1-1 transfers, C2 charges thru R1 and CR3.

3. Coin switch opens. After a short time delay due to C1 discharging thru R2 and K1 relay, K1 relaxes. C2 discharges thru relaxed relay contact K1-1 and energizes relay K2.

4. Relay contact K2-1 and K2-2 close causing the end ratchet to add 6 additional credits. After C2 discharge current has dissipated, K2 relay relaxes, K2-1 and K2-2 relay contacts open.

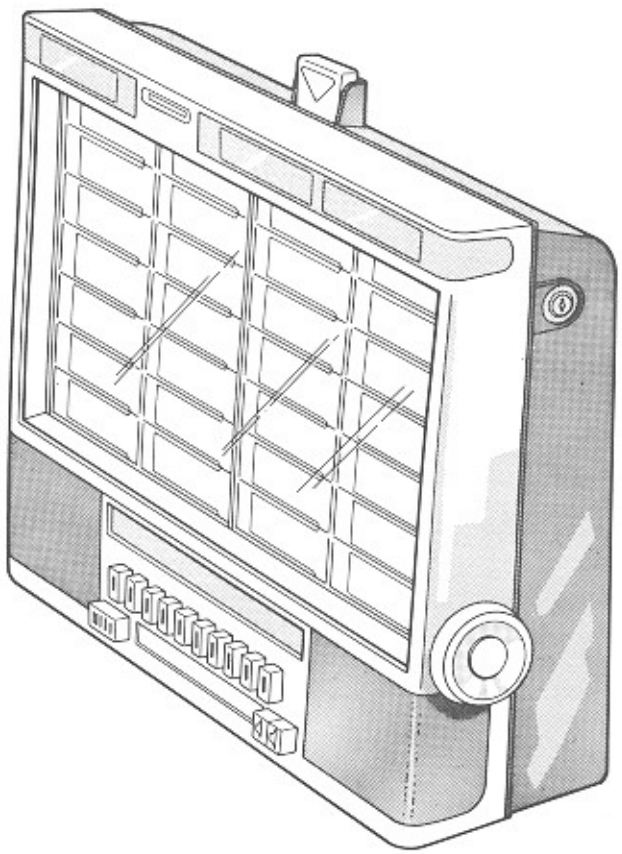
CYCLE OF OPERATION — 50 PFG

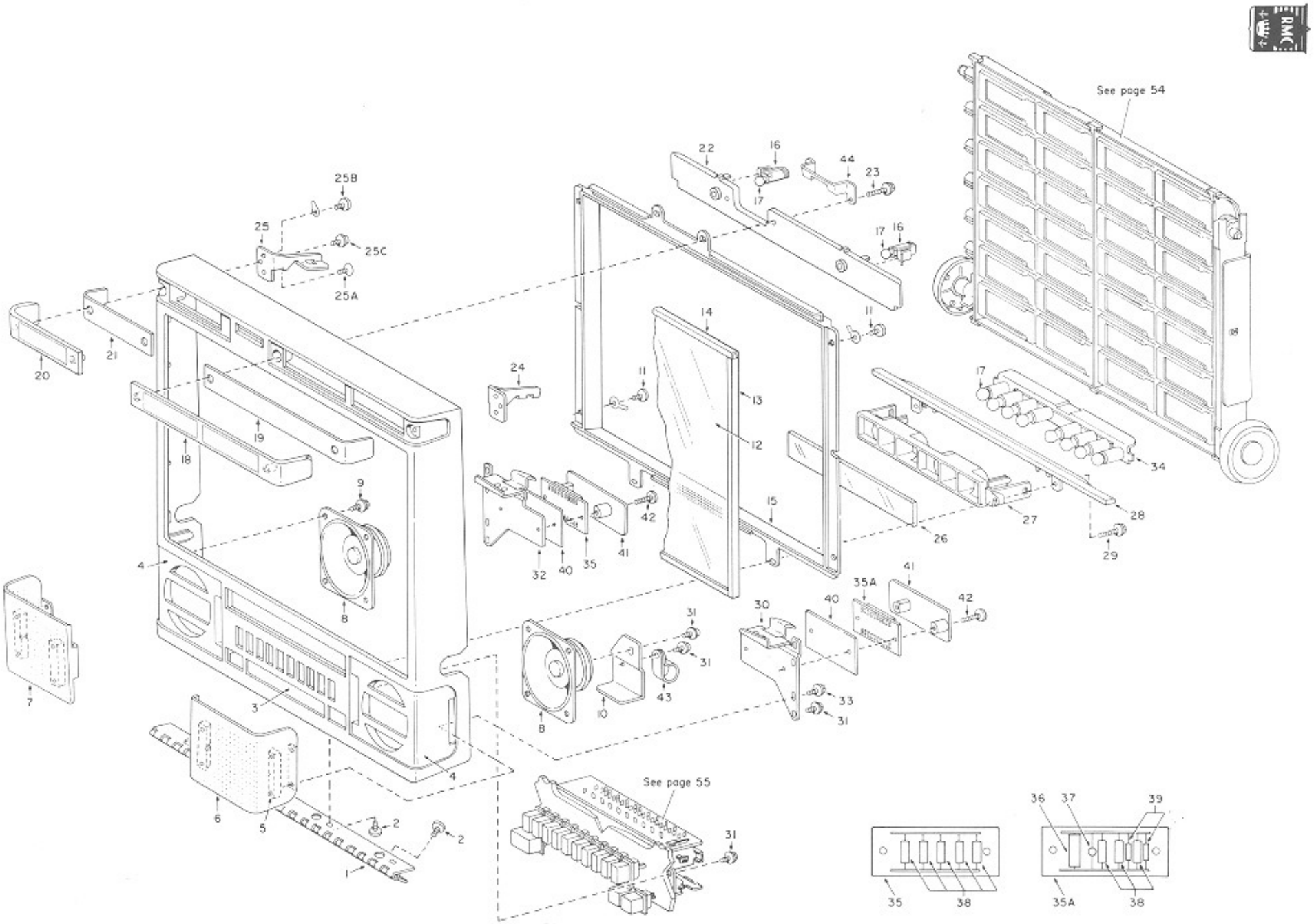
1. Down stroke of the 50 Pfg coin switch allows the master ratchet to register 1 credit via CR7; relay K1 energizes and C1 charges thru R2 and CR5.

2. Relay contact K1-2 transfers, C3 charges thru R3 and CR6.

3. Coin switch opens. After a short time delay due to C1 discharging thru R2 and K1 relay, K1 relaxes. C3 discharges thru the relaxed relay contact K1-2 and CR8 causing master ratchet to add one additional credit.

PARTS CATALOG SECTION




See page 54
See page 55
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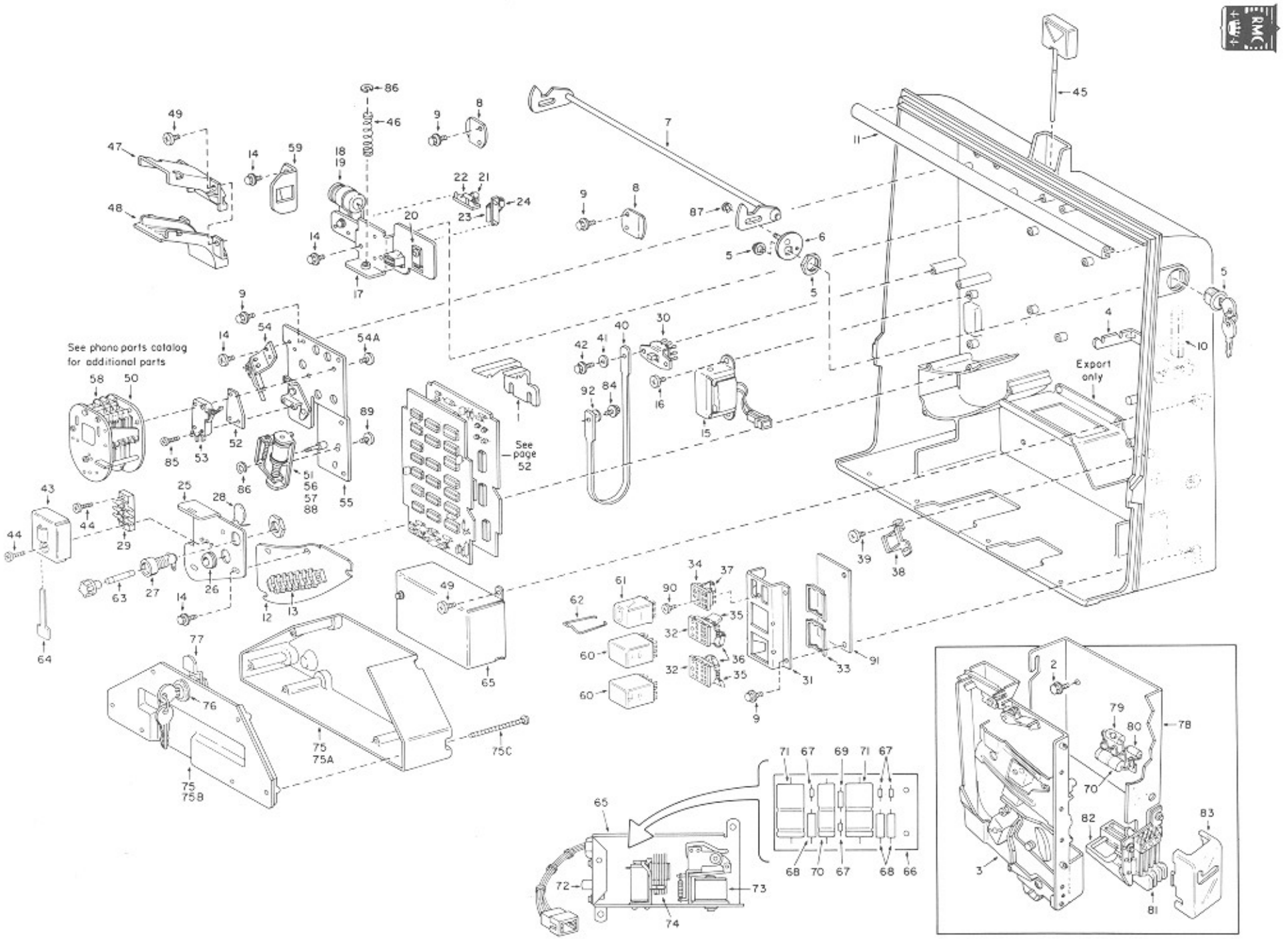
21
22
23
24
25
25A
25B
25C
26
27
28
29
30
31
32
33
34
35
35A
36
37
38
39
40
41
42
43
44

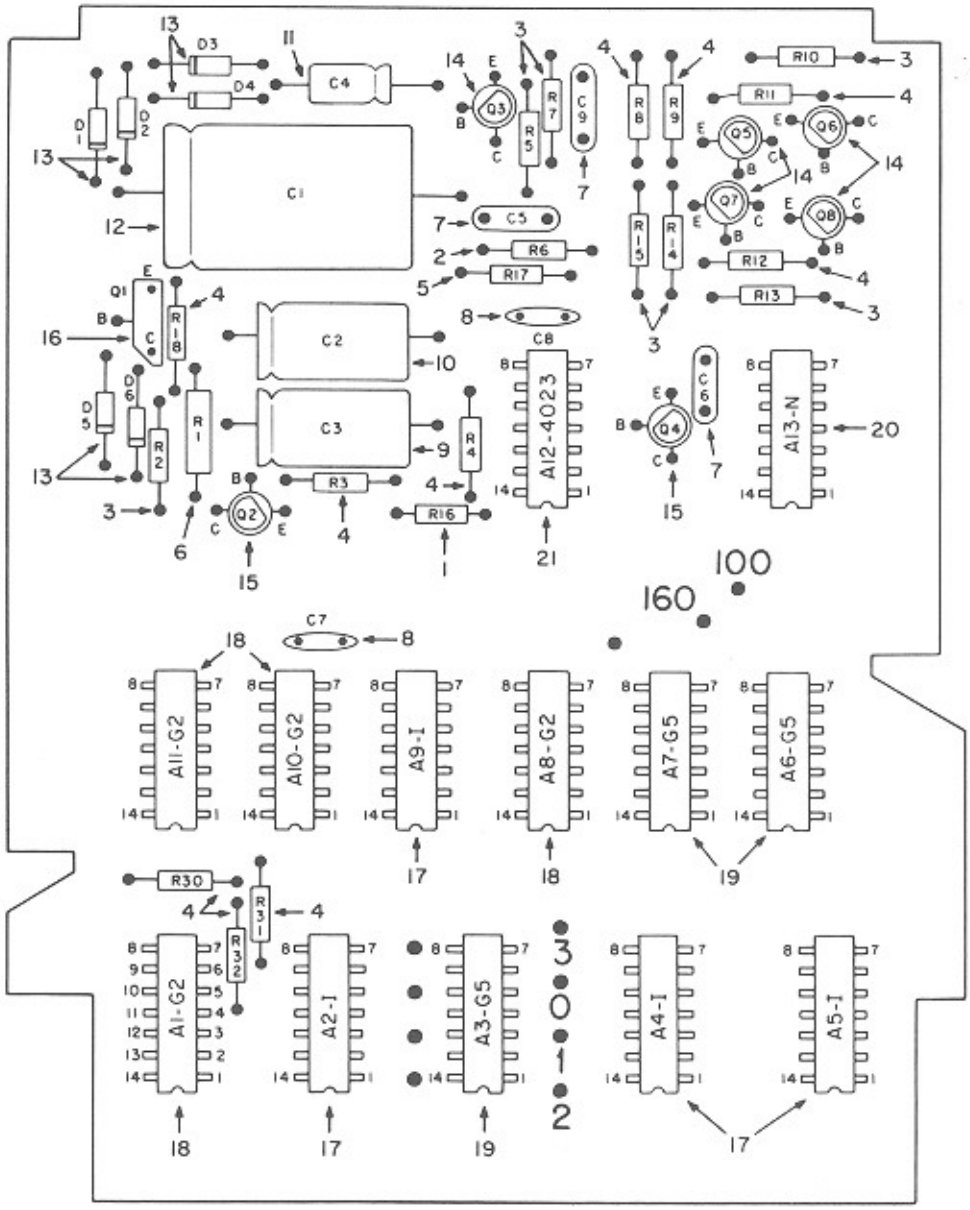
WALL BOX FRONT

Item	Part No.	Description	Item	Part No.	Description
1	47633	Hinge	25	47642	Bracket Lock L.H.
2	ST-10115	8-32x1/4 Ph. P.H.	25A	ST-10128	10-24x1/2 Phil Flat Hd.
3	47653	Insert – Wall Box Front	25B	ST-10051	10-24x1/2 Phil Pan Hd.
4	48093	Grille Liner	25C	ST-10129-D	8x13/16 Hex Washer Hd.
5	47608	Grille Retainer Block	26	47649	Signal Window (Domestic)
6	47629	Speaker Grille R.H.	27	47611	Light Box Signal Window
7	47631	Speaker Grille L.H.	28	47617	Light Diffuser – Lower Program
8	47637	"3" Speaker	29	ST-8274	8-32x7/8 Hex Flg.
9	ST-8268-D	8-32x5/16 Hex Flg.	30	48191-A	Program Mtg. Brkt. Assembly R.H.
10	48193	Cable Holder Bracket	31	ST-8269	8-32x3/8 Hex Flg.
11	ST-10130	8-32x3/8 Phil. Pan Hd.	32	48192-A	Program Mtg. Brkt. Assembly L.H.
12	47636	Front Glass	33	ST-10123-D	8x5/16 Hex Washer Hd.
13	47634	Vinyl Channel 1/8x8 7/8	34	47638-A	Light Channel & Socket Assembly
14	47634	Vinyl Channel 1/8x14 13/16	35	45828	10 Lug Terminal Board
15	47609	Program Shroud	35A	45828	10 Lug Terminal Board
16	48231-A	Light Socket Assembly	36	48048	22 Ohm 3 Watt Resistor
17	46739	#53 Bulb	37	47972	200 PRV Glass 1/5 Amp Rectifier
18	47604	Instruction Window Casting	38	14681	47 Ohm 1 Watt Resistor
19	47663	Instruction Card – Domestic	39	15686	470 Ohm 1/2 Watt Resistor
20	47606	Pricing Window Casting	40	45829	Insulator
21	47654	Pricing Card (2-25¢) LP	41	48207	Terminal Board Cover
22	47616	Light Diffuser Upper Program	42	ST-10081	6-32x3/4 Phil. Pan Hd.
23	ST-10129-D	8x13/16 Hex Washer Hd.	43	ST-3603	Black Nylon Clamp 9/16
24	47641	Bracket Lock R.H.	44	48076	Coin Slot Bracket (Export Only)


See phone parts catalog for additional parts
See page 52
Export only

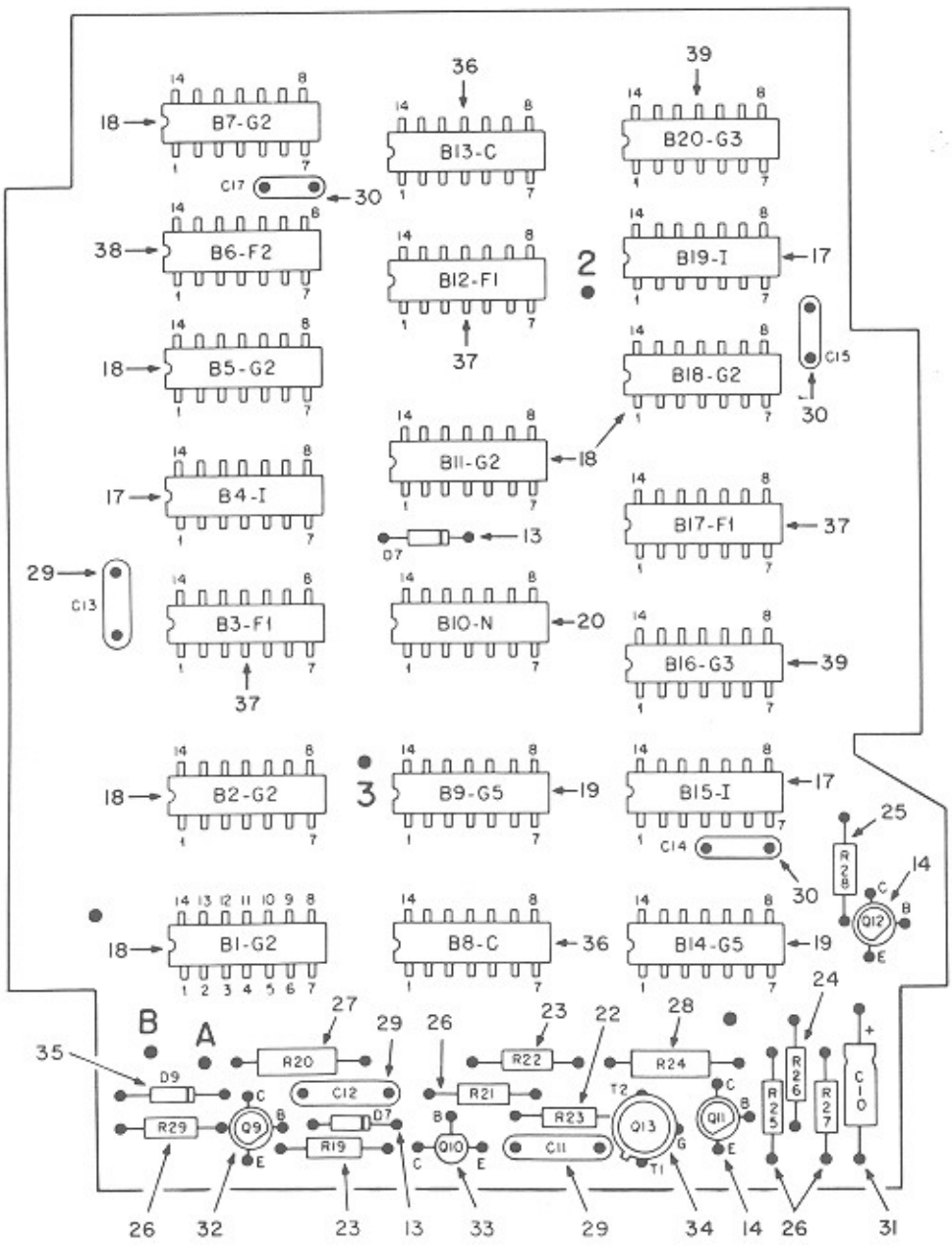
WALL BOX BACK

Item	Part No.	Description
1	47923	Spring
	ST-10134	Pop Rivet
2	ST-9733	4-40x1/4 Hex Flg.
3	47165	Rejector 50¢
4	47922	Mtg. Brkt.
5	ST-10086	Lock
6	48183-A	Cam Bolt Assem.
7	48184-A	Lock Bar Assem.
8	47931	Retainer
9	ST-8268-D	8-32x5/16 Hex Flg.
10	45816-4	Rubber Cushion
11	48224	Vinyl Channel
12	48242-A	Cover Assem.
13	47933	Terminal Block (7)
14	ST-8270-D	8-32x7/16 Hex Flg.
15	48194-A	Transformer Assem.
16	ST-10125	6-32x5/16 Pan Hd.
17	48146-A	Reject Brkt. Assem.
18	43536	250 Mfd. 64V. Cap.
19	ST-10119	Clamp 11/16
20	48103	Power Transistor
21	48101	5.6V. Zener Diode
22	31719	100 Ohm 1W Res.
23	16226	4.7K 1/2W Res.
24	48214	200 PRV 3 Amp Rect.
25	48241-A	Fuseholder Brkt. Assem.
26	14588	Rubber Grommet
27	47837	Fuseholder
28	45319	.02 Mfd. 100 WVDC Cap.
29	48136	Terminal Block (3)
30	37420	Switch
31	47907	Relay Brkt.
32	44806	Relay Socket
33	44807	Retainer
34	47471	Relay Socket
	ST-6577	4-40x1/4 Phil. Pan Hd.
35	47421	.1 Mfd. 250 WVDC Cap.
36	35632	220 Ohm 1/2W Res.
37	46497	100 PRV 1 Amp Rect.
38	48139	Plug Brkt. (15)
39	ST-8266	8-32x5/16 Phil. Pan Hd.
40	48134	Hinge Stay
41	ST-332	Flat Washer
42	8259-D	6-32x7/16 Hex Flg.
43	48208	Terminal Cover
44	ST-7248	4-40x1/2 Phil. Pan Hd.
45	47607	Reject Button
46	37054	Return Spring
47	47612	Coin Chute – Upper
48	47613	Coin Chute – Lower
49	ST-8277	8-32x7/16 Phil. Pan Hd.
50	39655-4A	Accumulator Assem.
51	37664-A	Reset Pawl Assem.
	37567	Pawl Guide
	17982	Pawl
	14028	Spring
52	40811	Shim
53	39611	Switch
54	34000-1A	Control Sw. & Brkt. Assem.
54A	ST-4559	6-32x3/16 Phil. Pan Hd.
55	37616-1A	Accum. Mtg. Plate Assem.
56	37600-1	Reset Coil
57	37634-A	Reset Coil Brkt. Assem.
	37556	Reset Coil Brkt. (Rear)
	39784	Armature Back Stop
	36555	Reset Coil Brkt. (Front)
	37570	Reset Armature
	34559	Return Spring
58	46497	100 PRV 1 Amp Rect.
59	47903	Plug Brkt.
60	45305	Relay – 24 VAC
61	47386-1	Relay – 24 VDC
62	48176	Spring
63	ST-4332	1 Amp Slo Blo Fuse
64	37392	Seal
65	47650-A	2/3 Quarter Adapter
66	48142-A	P.C. Brd. Wiring Assem.
67	46497	1 Amp Min. Sil. Rect.
68	38713	12 Ohm 1W Res.
69	35632	220 Ohm 1/2W Res.
70	41501	100 Mfd. 64V Cap.
71	43536	250 Mfd. 64V Cap.
72	40510	Slide Switch
73	45831	Sequence Relay
74	41502	Relay
75	48132-A	Cash Box Assem. (Dom.)
75A	48128	Cash Box Back
75B	48131	Cash Box Front
75C	ST-10093	#6x2" Hex Flg.
76	ST-7411	Lock (Export)
77	47915	Cam Bolt (Export)
78	48144-A	Reject Housing Assem.
	48147-A	Reject Housing (Export)
79	47972	200 PRV Silicon Rect.
80	33248	47 Ohm 1W Res.
81	48078-A	Coin Switch Assem. (50¢)
	48079-A	Coin Switch (Export)
82	45460	Coin Guide
q	ST-9728	4-40x1/4 Phil. Pan Hd.
83	45463-1	Coin Switch Cover
84	ST-8269	8-32x3/8 Hex Flg.
85	ST-6526	2-56x7/16 Pan H.M.S.
86	ST-9825	Keeper
87	ST-9263	Retaining Ring
88	ST-7233	6-32x5/16 Phil. P.H.M.S. (Brass)
	ST-3417	Keps Nut
89	ST-4555	6-32x1/4 Phil. P.H.M.S.
90	ST-6577	4-40x1/4 Phil. P.H.M.S.
91	47924	Insulator
92	ST-4881	Flat Washer



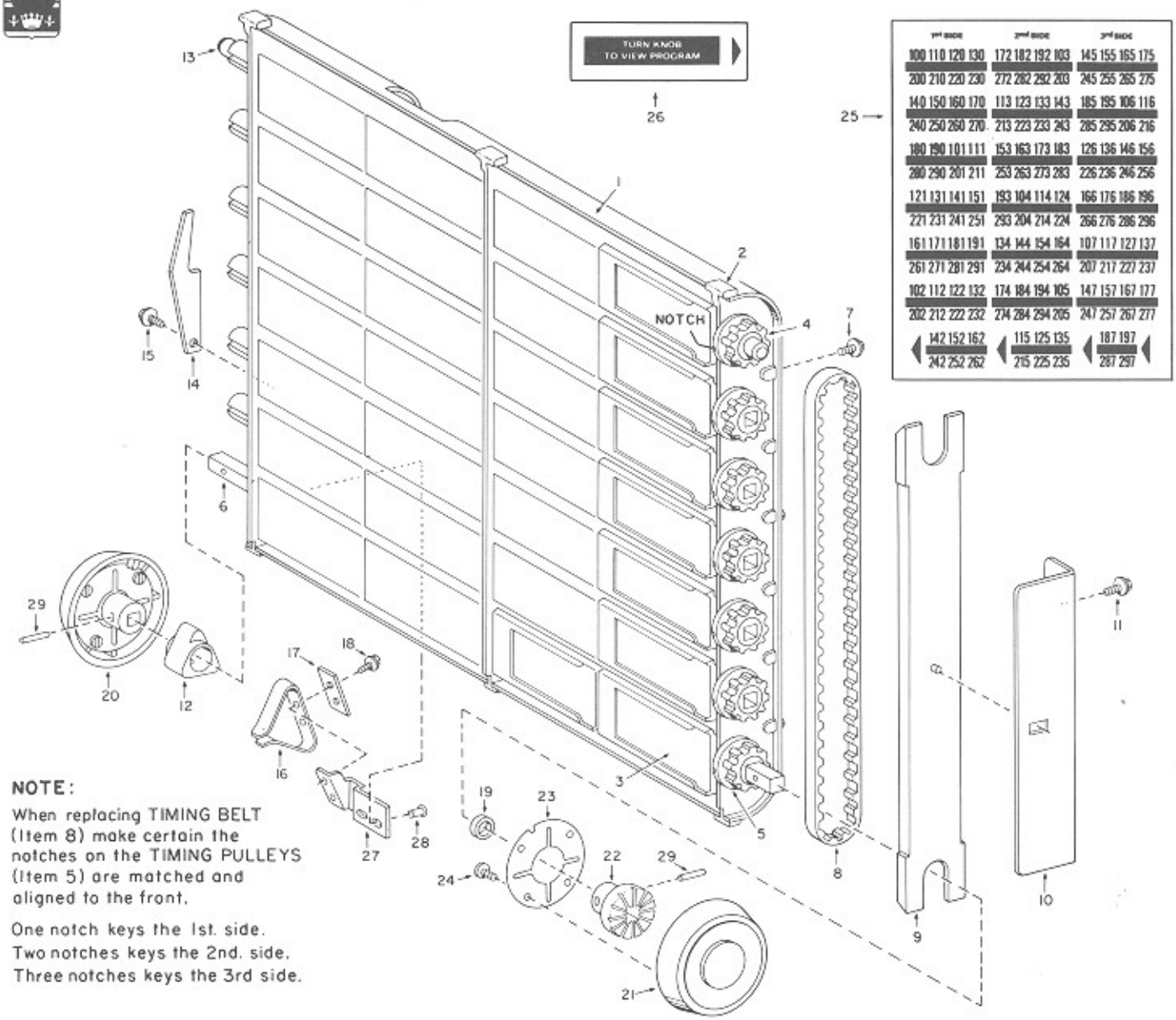
P.C. BOARD No. 1 (BOTTOM) — No. 47660-A

Item	Part No.	Description	Item	Part No.	Description
1	48042	2200 Ohm 1/4 Watt Resistor	10	48037	47 Mfd 50 WVDC Capacitor
2	48043	4700 Ohm 1/4 Watt Resistor	11	48038	20 Mfd 16 WVDC Capacitor
3	48044	10K Ohm 1/4 Watt Resistor	12	48039	1000 Mfd 25 WVDC Capacitor
4	48046	22K Ohm 1/4 Watt Resistor	13	46497	100 Prv Silicon Rectifier
5	48047	470K Ohm 1/4 Watt Resistor	14	48063	2N5307 Transistor
6	32831	2200 Ohm 1/2 Watt Resistor	15	45747	2N4424 Transistor
7	47421	.1 Mfd 250 WVDC Capacitor	16	45746	D40A13 Silicon Power Tab Trans.
8	45791	2200 Pf Ceramic Disc Cap.	17	48051	Dtl Hex Inverter
9	45313	32 Mfd 64 WVDC Capacitor	18	48053	Dtl Quad. 1-Input Nand Gate



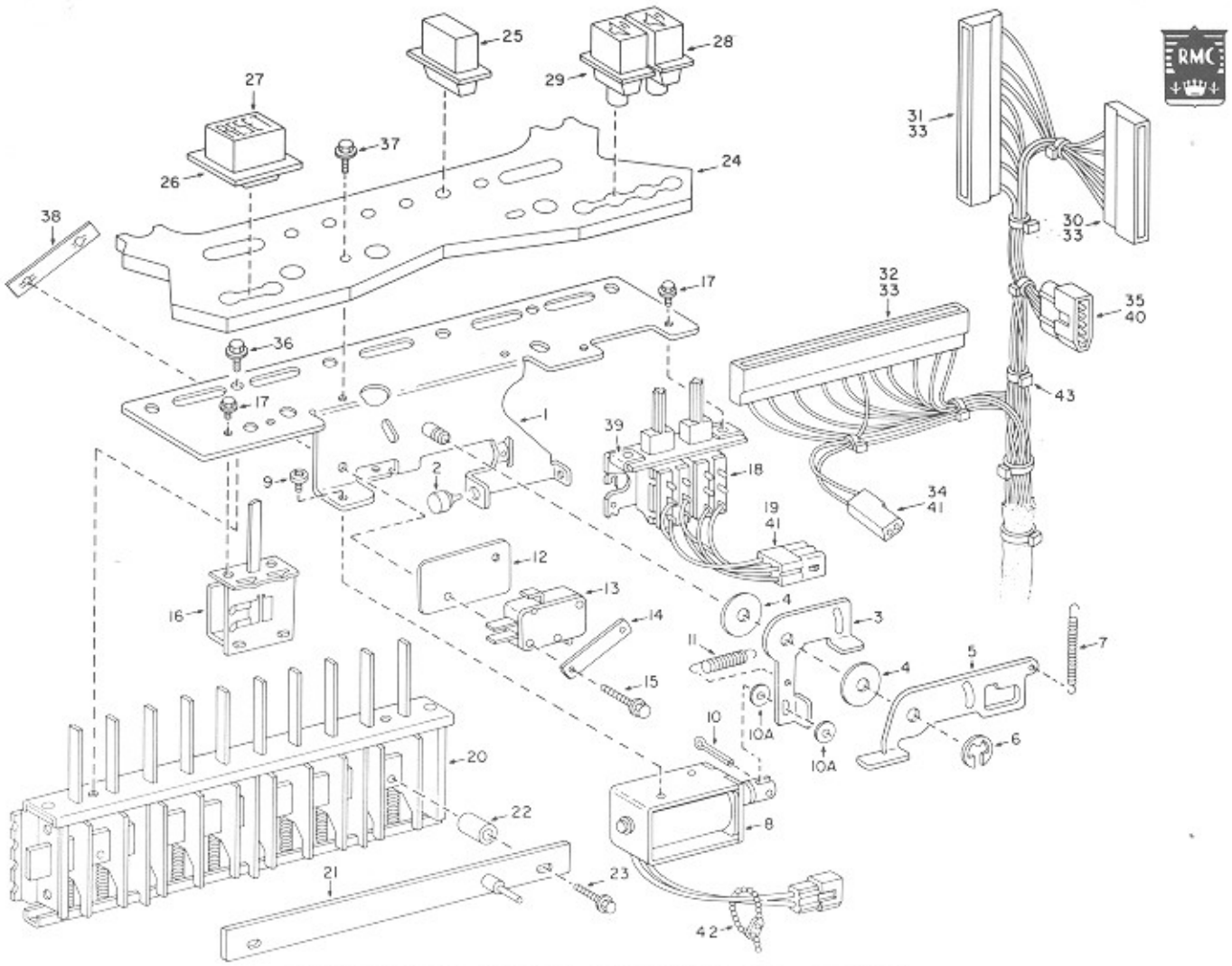
P.C. BOARD No. 2 (TOP) — No. 47665-A

Item	Part No.	Description	Item	Part No.	Description
19	48058	Dtl Dual 5 — Input Nand Gate	30	47723	680 Pf Ceramic Disc Capacitor
20	48059	Dtl Quad. 2 — Input Nor Gate	31	48036	10 Mfd 16 WVDC Capacitor
21	48061	Ttl 4-Bit Universal Counter	32	43548	2N3417 Transistor
22	48041	100 Ohm 1/4 Watt Resistor	33	47831	MPSA56 Transistor
23	48042	2200 Ohm 1/4 Watt Resistor	34	48064	2.5 Amp Triac
24	48044	10K Ohm 1/4 Watt Resistor	35	48108	56 Volt Zener Diode
25	47832	5600 Ohm 1/4 Watt Resistor	36	48052	Dtl Divide By 16 Counter
26	48046	22K Ohm 1/4 Watt Resistor	37	48054	Dtl Dual J-K Flip-Flop
27	36287	56 Ohm 1/2 Watt Resistor	38	48056	Dtl Dual J-K Flip-Flop
28	35696	270 Ohm 1/2 Watt Resistor	39	48057	Dtl Triple 3-Input Nand Gate
29	47421	.1 Mfd 250 WVDC Capacitor			



PROGRAM HOLDER ASSEMBLY — No. 47610-A

Item	Part No.	Description	Item	Part No.	Description
1	48187-A	Program Frame Assembly	16	47643	Program Detent Spring
2	47593	Program Bearing	17	48123	Support Plate
3	46975	Program Holder	18	ST-2546	5-40x1/4 Hex Flg.
4	48188-A	Pulley & Guide Pin Assem.	19	48091	Program Spacer
5	47592	Timing Pulley	20	48190-A	Program Knob Assembly
6	47621	Program Shaft	21	47602	Program Knob Only—Outer
7	ST-10123	8x5/16 Hex Washer Hd.	22	47603	Program Knob—Inner
8	47596	Timing Belt	23	47622	Knob Clutch Spring
9	47591	Program Belt Retainer	24	ST-4041	6x1/4 Phil Pan Hd.
10	47644	Retainer Bracket	25	47672	Number Strips (Set)
11	ST-9743-D	8x3/8 Hex Washer Hd.	26	47667	View Program Card (Dom.)
12	47601	Program Detent	27	48089	Detent Bracket
13	47937	Program Guide Pin	28	ST-979	1/8 Dia. x 3/16 Rivet
14	47619	Program Lock	29	ST-255	3/32 Dia. x 5/8 Roll Pin
15	ST-8298	8x1/2 Hex Washer Hd.			



PUSH BUTTON SWITCH ASSEMBLY — No. 47615-A

Item	Part No.	Description	Item	Part No.	Description
1	47938-A	Solenoid Mtg. Plate Assem.	22	47132	Spacer
2	ST-2320	Solenoid Bumper	23	ST-2560	6-32x5/8 Hex Flg.
3	47136	Solenoid Lever	24	47614	Light Diffuser
4	47138	Lock Lever Washer	25	47002	Button Set (1 Thru 0)
5	47133	Locking Lever	26	47599	Reset Button
6	ST-9245	Truarc "E" Ring	27	47646	Button Insert
7	35109	Rocker Bar Spring	28	47597	Button — Soft
8	48219-A	Solenoid Assembly	29	47598	Button — Loud
9	ST-6335	6-32x3/16 P.P.H.	30	46734	Edge Connector — 12 Cir.
10	ST-1024	Cotter Pin (Stainless)	31	48106	Edge Connector — 18 Cir.
10A	ST-9430	Fiber Washer	32	48107	Edge Connector — 24 Cir.
11	47134	Return Spring	33	46733	Contact
12	43494	Insulator	34	48149	2 Cir. Min. Recept.
13	42397	Micro Switch	35	48151	5 Cir. Min. Recept.
14	45395	Hold Down Plate	36	ST-2566	8-32x1/4 Hex Flg.
15	ST-8286	4x3/4 Hex Flg.	37	ST-8269	8-32x3/8 Hex Flg.
16	47128	Reset Switch	38	ST-10117	Speed Nut
17	ST-2555	6-32x1/4 Hex Flg.	39	ST-10118	Speed Nut Fastener
18	47127	Tone Switch	40	48116	Pin
19	48153	6 Cir. Min. Recept.	41	48114	Socket
20	47126	Push Button Switch	42	ST-9248	Wire Tie
21	48182-A	Lock Bar Assembly	43	ST-10122	Sta-Strap

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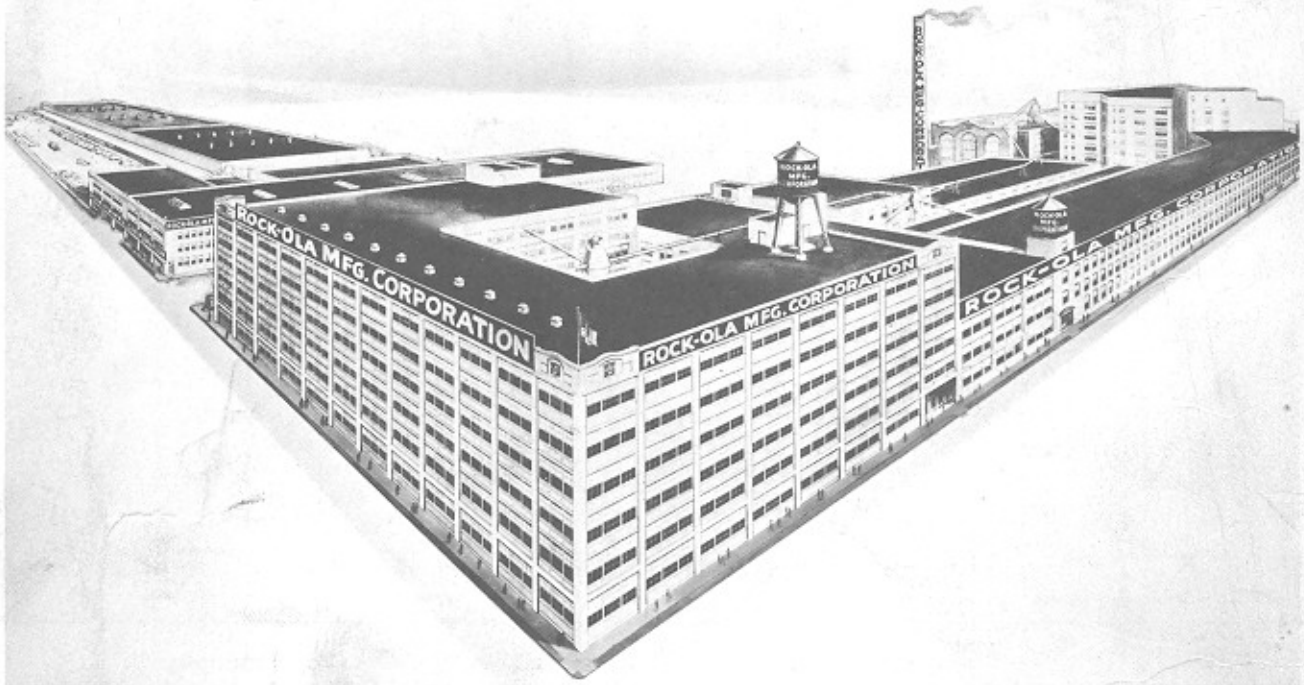

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